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Pinned-surface and double-junction photodiode type super high-performance image sensor with built-in solar cell structure

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Highlights:

- Semiconductor band theory of silicon-based double and triple Junction type photodiodes.
- Electron/hole pair separation enhanced by surface conduction band bending in surface P+P hole accumulation region.
- Energy spectrum density and penetration depth of Sun light into silicon crystal.
- Maximum Power Tracking Technology (MPTT) on pinned-surface double-junction photodiode type solar cell.
- Floating-surface hole/electron recombination loss of the conventional single junction type solar cell.

Abstract: Floating surface single-junction type photodiodes are mostly used in solar cell applications for simplicity and cost. On the other hand, pinned-surface and double-junction type photodiodes are used now in super high-performance image sensor applications. This paper first reviews the difference between the conventional floating-surface single-junction type photodiode and the pinned-surface double-junction type photodiode. The pinned-surface buried-channel P+PNPP+ double junction type photodiodes are very high-performance image sensors with no image lag and very high light sensitivity compared to conventional ones. The diode can be applied not only to image sensors but also to solar cells. In addition, this paper proposes a new AI robot vision chip in the modern 3DIC CMOS image sensor technology using this double junction type diode. So, the diode will be widely interested in process, device, and application researchers and engineers for image sensors and solar cells. A real-time AI smart robot vision chip is described as an example of application, which is composed of an array of N × N pinned-surface buried-channel P+PNPP+ double junction type photo diodes, N × N analog-data stream mask-and-match comparators, digital processing and SRAM cache buffer memory units, integrated in a 3-D multichip architecture. In the external power-off mode, the image sensor array of N × N pinned-surface buried-channel P+PNPP+ double junction type photo diodes also function as a solar cell unit for the AI self-energy robot vision chip.

Keywords: pinned-surface; floating-surface; depletion width; image sensor; solar cell; energy efficiency; maximum power tracking technology; multi digital bit data comparator; 3DIC multichip

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1. Introduction

Charge couple device (CCD) type charge transfer device (CTD), originally invented in 1970 [1], is composed of a series of MOS large-capacitor gates, and consumes a large power for charging and discharging the large CCD/MOS capacitors in order to perform the complete charge transfer operations. Thanks to the advancements in the long history [2–9] of modern low-power CMOS process scaling technology, CCD type CTD is now completely replaced by the low-power digital CMOS type CTD with the in-pixel source-follower current-amplifier circuit originally invented by Peter Noble in 1969 [10]. Since the size of the source-follower current amplifier circuit was too large to be included in each pixel, the buried-channel charge coupled device (CCD) type charge transfer device (CTD) [11–13] was used till late 1990s. Thanks to the modern CMOS scaled advanced process technology, in our high-definition digital TV era, MOS transistors and S/D contacts have now become small enough to be included in each pixel of image sensors. Charge Coupled Device (CCD) type was not the only charge transfer device (CTD) that transfers the information of one single photo electron for a long distance in a silicon chip. Image sensor in general is composed of three basic parts, (1) a light-sensing photodiode, (2) a signal charge transfer device (CTD) and (3) the image information processing unit as shown in Figure 1a.

Historically, the first original PNP double junction buried-channel type light-sensing photodiode was invented by Philips in Netherland on June 9, 1975 [14] as shown in Figure 1b. The dashed line in the figure shows the empty potential well in the buried channel for a single electron to move along for a long distance in the silicon chip. However, the surface P region was connected only to the high-resistivity substrate, with some undesired RC delay time to the substrate pinned ground voltage level. This device works only for low-frequency operations because of the RC delay time constant to the substrate.

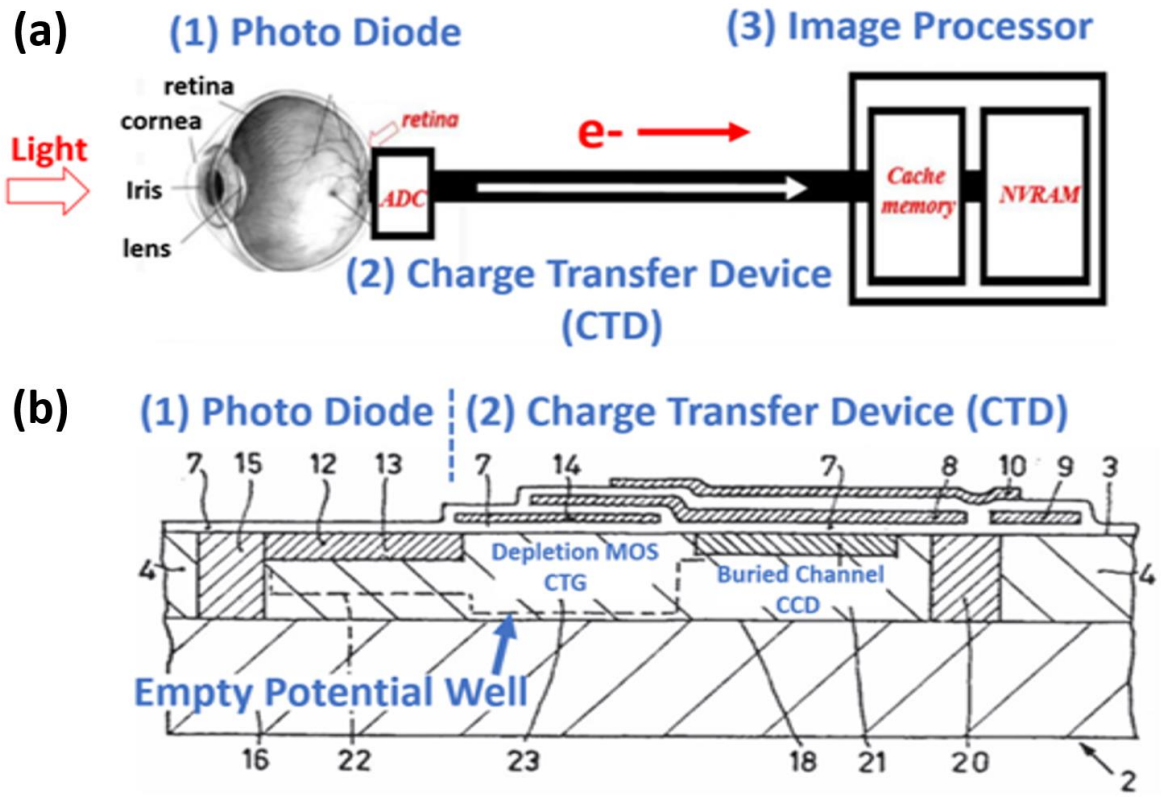

Figure 1. (a) an image sensor unit diagram and **(b)** a double-junction photodiode by Phillips.

Figure 2 shows the pinned-surface completely-majority-carrier-depleted charge-collecting buried-channel/storage region with the complete charge transfer capability for high-frequency operations, realizing the completely-mechanical-free film-less Global and Electrical Shuter functions. At low frequency, the surface P-region can remain grounded and the buried N-region can be kept completely depleted of the majority carrier electrons. And with no minority carrier hole present for recombination in the buried N-channel region, this PNP double junction photodiode can transfer one single photo electron for a distance inside of the silicon chip without recombination at low frequency. For high frequency operations, however, the surface hole accumulation region must be pinned in order to function as a pinned virtual gate for realizing the no-image-lag feature with the high-frequency global and electronic shutter function capability, in order to realize high-performance video camera operations, completely free from any mechanical parts and any film media. The difference between the pinned-surface and the floating-surface photodiodes makes a big difference [15]. High performance pinned-surface double and triple junction photodiodes invented by Hagiwara at Sony in 1975 were hinted by Sony original double and triple junction type bipolar dynamic transistor technology [16]. They had a unique in-pixel vertical overflow drain (VOD) built-in structure with the global and electronic shutter capability, suitable for consumer video camera applications. See Figure 2. Sony filed in 1975 a series of Japanese patent applications on the in-pixel pinned-surface and buried-channel double and triple junction photodiodes, but never disclosed the details until recently [17–19]. Sony pinned-photodiodes have the unique global and global shutter capability for capturing quick action pictures, free from any mechanical parts and replacing completely the film media by electronic media. A high-energy ion implantation technology with a unique lamp anneal method [20] was used to fabricate the pinned-surface P+PNPP+ double junction photodiode. Sony reported the complete charge transfer capability and the high quantum efficiency in the SSDM1977 and the SSDM1978 international conferences, and also in another domestic conference in Tokyo. Then, Sony was invited to talk at the CCD1979 conference in Edinburgh, Scotland UK and also at the ECS1980 conference in St. Louis, USA. In 1979, Hynecek developed a virtual-phase CCD delay line with the complete charge transfer capability with the pinned-surface buried-channel PNP junction photodiode [21]. The pinned-surface of the PNP junction photodiode functions as a virtual gate for the complete charge transfer action. In 1982 NEC developed the buried-channel photodiode and used it in an ILT CCD type CTD image sensor with detailed measurement data of the image lag [22–23]. The NEC photodiode, used in the ILT CCD, reported in IEDM1982 was identical with the Philips 1975 invention of the floating-surface PNP double junction buried photodiode. The surface hole accumulation was connected to the high resistivity substrate. In IEDM1984, Kodak emphasized the importance of the pinning the surface hole accumulation region to achieve the completely-no-image-lag feature. Kodak reported that there was no image lag and named the device as Pinned Photodiode [24], which is now widely known as the pinned-surface photodiode. The SSDM1978 conference paper by Sony and the IEDM1984 conference paper by KODAK both reported the excellent short-wave blue-light sensitivity with a very high quantum-efficiency of 60–80% on image sensor chips. The CCD type charge transfer device (CTD) is now completely replaced by the in-pixel source-follower current-amplifier circuit, originally invented in 1969 by Peter Noble, owing to the advancements of the scaled modern digital CMOS process technology. However, the pinned-surface buried-channel P+PNPP+ double junction photodiode, invented in 1975 by Sony, has been used in the CCD video cameras in the analog TV era and also now widely in CMOS video cameras and smart phones in our modern digital TV era.

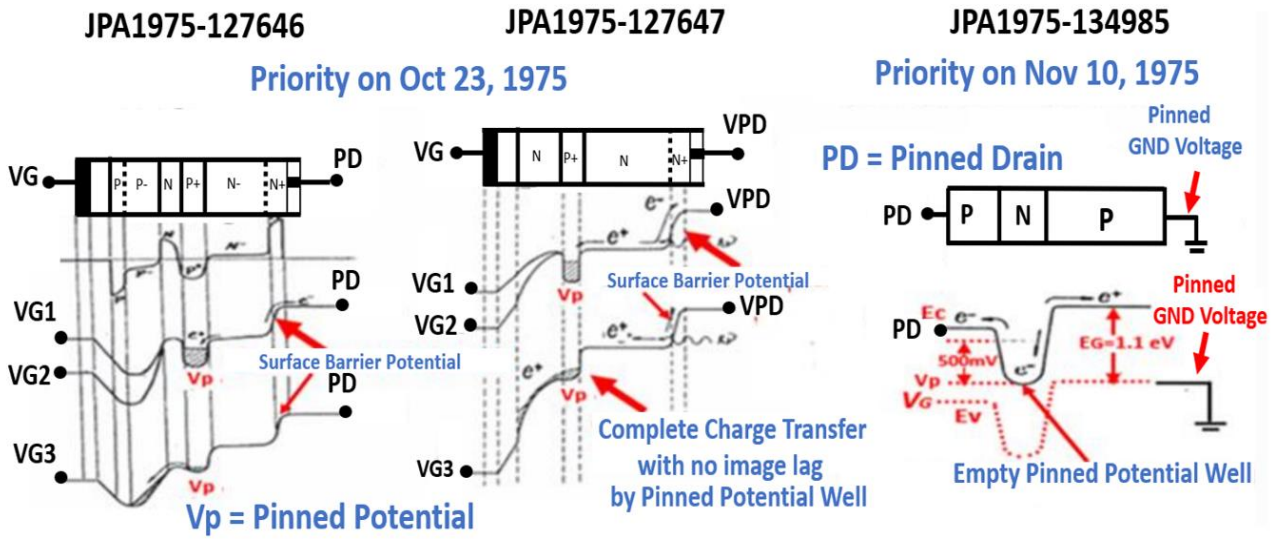

Figure 2. Pinned-surface completely-depleted buried-channel double and triple junction photodiodes invented by Yoshiaki Hagiwara at Sony in 1975, later named as Pinned Photodiode by Kodak in 1984 and Hole Accumulation Diode (HAD) by Sony in 1989.

2. Multi-chip 3DIC back-light illuminated CMOS image sensor for real-time AI robot vision

In Figure 3, a smart vision chip now proposed by the author is explained in details, which is based on the original architecture of a multi-bit digital-data comparator processor [25], a real-time high-performance digital engine, which was taught in the 1972 Caltech Digital Circuit Design Course, and was fabricated in the Intel 1972 Enhancement and Depletion (E/D) MOS process technology. Under the guidance of Prof. C. A. Mead at Caltech, his EE graduate students designed the chip. It was a R/D project under the collaboration of a university and an industry for the first time in the world.

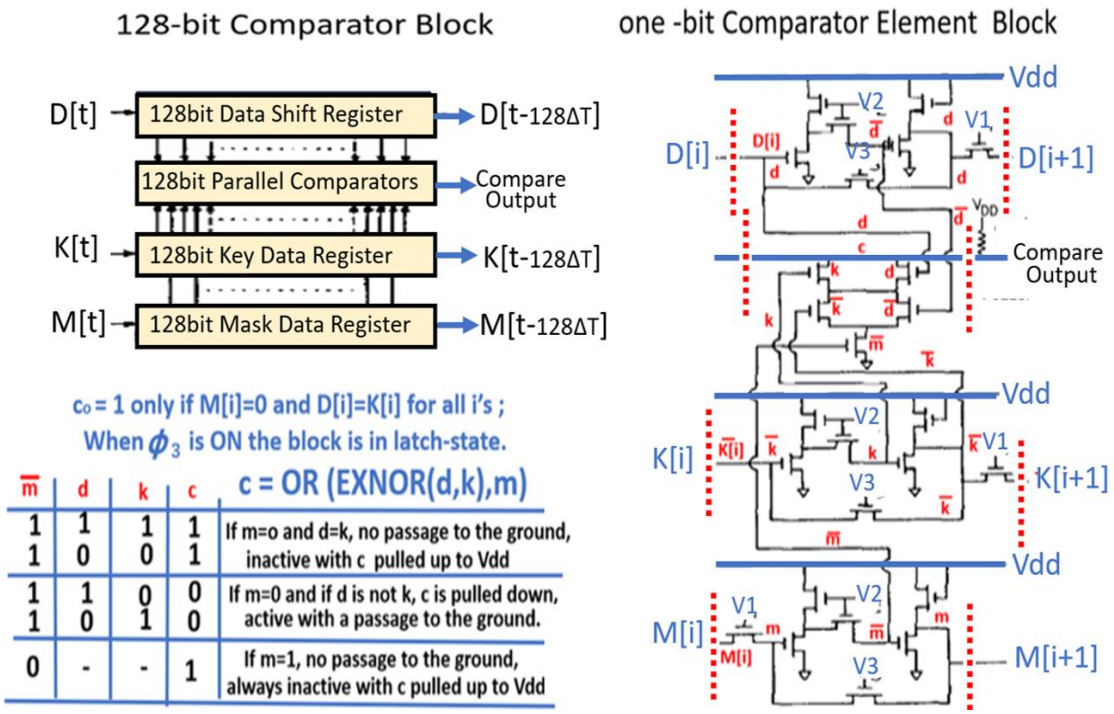

Figure 3. Full schematics of one bit slice of a new 128-bit multi-comparator for AI robot vision.

Based on the early works [26–28], Sony now has advanced CMOS scaled process and 3DIC multi-chip complex packaging technology for realizing real-time smart robot vision chips. Figure 4 shows a cross-sectional view of a newly proposed smart robot vision chip by the author in 3DIC multichip architecture [29–33]. A real-time AI smart robot vision chip is now proposed as a new application in this paper, which is composed of the N ×N analog-data steam mask-and-match comparators developed in 1972 by Caltech students, an array of N × N pinned-surface buried-channel P+PNPP+ double junction type photo diodes invented in 1975 by Sony, and a high-speed cache SRAM buffer memory unit [34], originally developed for all-solid-state digital cameras. All of them are integrated in a 3DIC multichip.

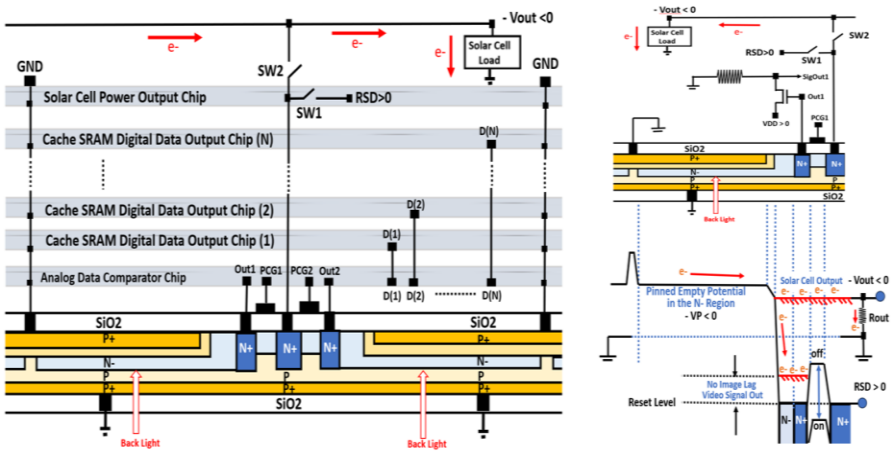

Figure 4. A cross-sectional view of a new AI Robot Vision chip in 3DIC multichip architecture.

Figure 5 shows one-pixel unit of a unique high-performance image sensor unit, with the solar cell capability, which is composed of a pinned-surface buried-channel P+PNPP+ double junction photodiode with an in-pixel source-follower current-amplifier, and also with a depletion MOS type charge transfer gate (CTG) and another depletion MOS type pre-charging gate (PCG) with a switching outlet diffusion drain (ODD) region, for draining out the photo signal electrons. When in use for energizing the solar cell load, we have $SW1 = off$ and $SW2 = off$. When not in use, we have $SW1 = off$ and $SW2 = off$.

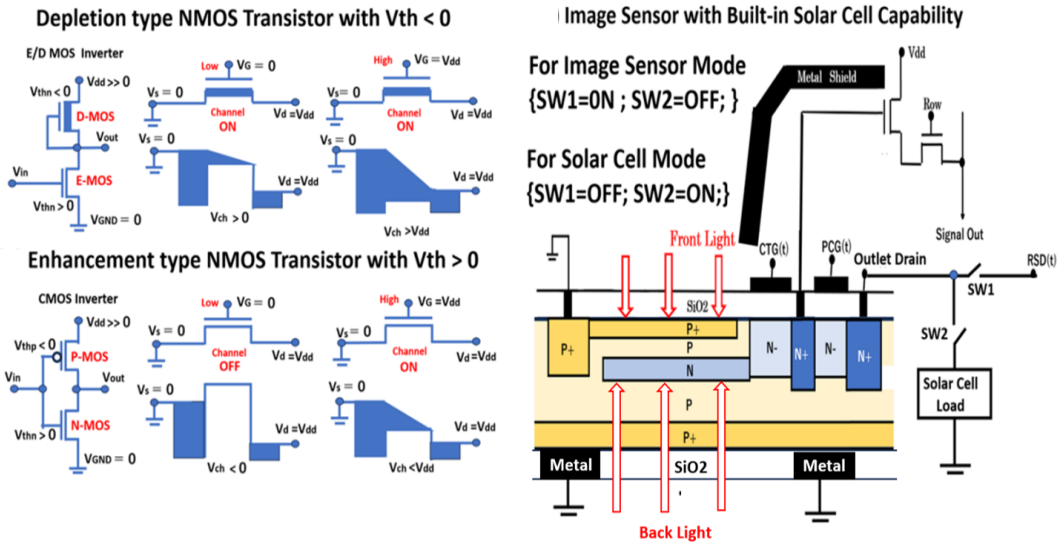

Figure 5. Active pixel image sensor with Depletion type CTG and PCG MOS Transistors.

3. Difference of floating-surface single junction and pinned-surface double junction photodiodes

Figure 6 shows a circuit model of (a) the floating-surfacer N+NPP+ single-junction-type solar cell and (b) the new pinned-surface P+PNPP+ double-junction-type solar cell.

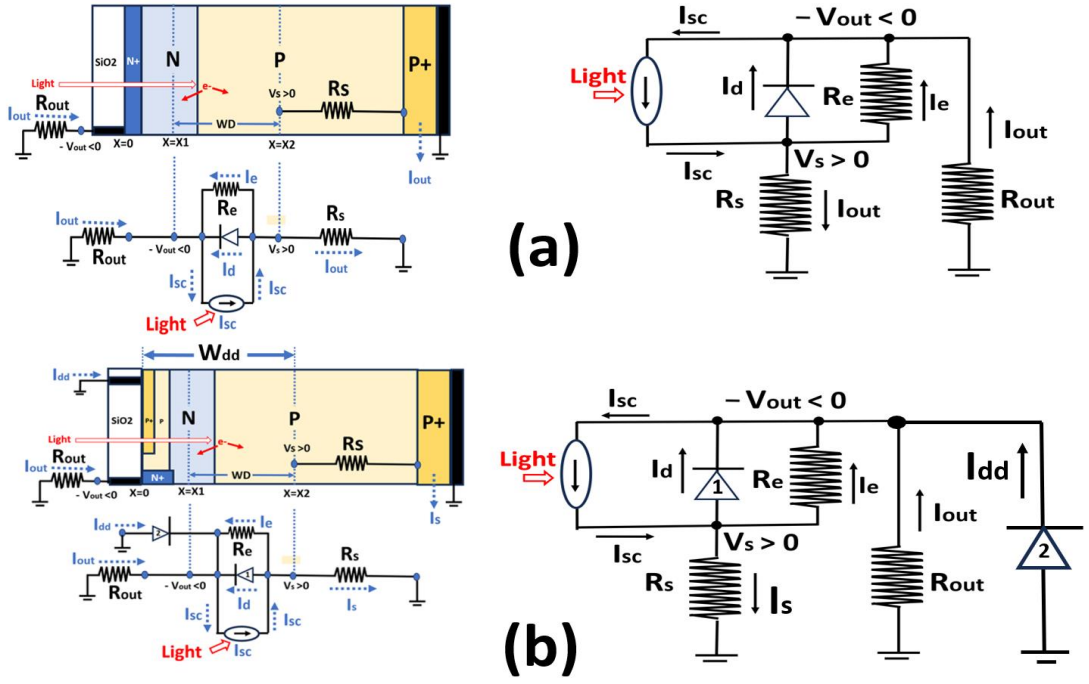

Figure 6. A circuit model of **(a)** the floating-surfacer N+NPP+ single-junction-type solar cell and **(b)** the proposed pinned-surface P+PNPP+ double-Junction solar cell in comparison.

In case of the floating-surface N+NPP+ single junction solar cell, the input solar cell current Isc is given as (1) $Isc = Id + Iout + Ie$ while the output voltage Vout is given as (2) $Vout = (Iout)(Rout)$ and the large P-type substrate resistance Rs is related with the output current Iout as (3) $Vs = (Iout)(Rs)$.

The small photo diode leakage current Ie is given as (4) $(Vs + Vout) = (Ie)(Re)$ while the photo diode forward current Id is given as (5) $Id = Io\left(exp\left((Vout + Vs)/kT\right) - 1\right)$;

There are five equations (1) through (5) with five unknown parameters {Vout, Vs, Id, Ie, Iout} which can be determined uniquely with the input independent parameters {Isc, DP, DN, Re, Rs, Rout}. By applying the maximum power tracking technology (MATT), the solar cell output power (Iout)(Vout) can be maximized by controlling the output solar cell voltage Vout.

The values of VBP and VBN determine uniquely values DP and DN respectively. We obtain then value of VB by the relation $VB = EG - Vout - VBP - VBN$. the depletion width WD is uniquely determined as $WD = sqrt\left((2\varepsilon_{si}VB)(DP)(DN)/(DP + DP)\right)$.

The maximum allowed width Wdd of about 2 of the depletion region WD for the N+PPsub single junction type solar cell is easily obtained numerically solving the set of these non-linea equations, (1) through (5). When the doping level DN of the surface N-region approaches the limiting value of the state density Nc of the conduction band edge, we have $VBN \to 0$. We have $VB = EG - VBP - Vout$ since we have the relationship $EG = Vout + VB + VBN + VBP$. When both the doping level DP of the P-type substrate wafer and the doping level DN of the surface N-region approach zero, the barrier potentials VBN and VBP both approach to EG/2 respectively.

And the sum of the barrier potentials (VBN+VBP) approaches the silicon band gap energy EG. As shown in Figure 7, we then have $Vout \to 0$; $VB \to 0$. A intrinsic semicondutor or an extremely-low-concentration semiconductor wafer resulting in a very large delpletion width Wd for effective separations of photo electron and hole pairs. The N+P junction photodiodes with the floating-surface N regions suffer undesired serious image lag problem. For intrinsic silicons used in the photodiode Fermi level Ef approaches to the middle of the silicon band gap. As explained in details later, the external metal-to-semiconductor ohmic contact formation with the intrinsic semiconductor induces an undesired voltage drop, lowering the output voltage.

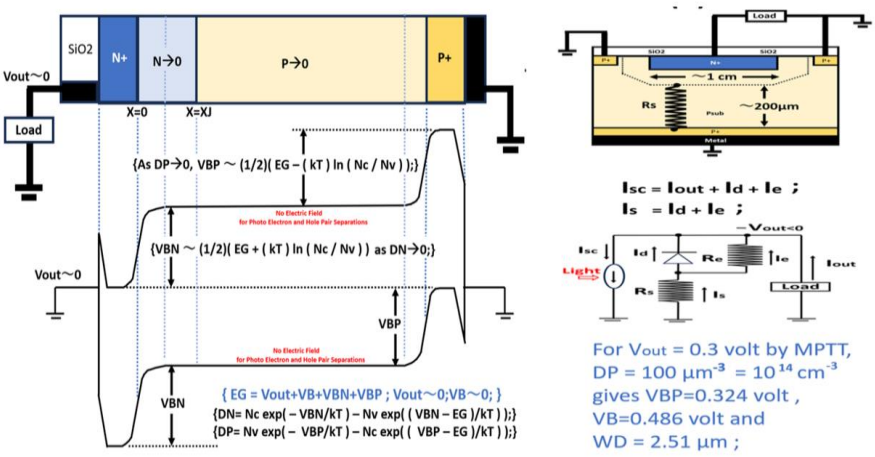

Figure 7. A Floating-Surface N+NPP+ Single Junction Photodiode Solar Cell as $DP \to 0$ and $DN \to 0$.

Figure 8 shows various types of photodidoes in comparison for solar cell applcations, such as (1) the classical very simple conventional floating-surface N+P single junction photo diode, now widely used for solar cell applications with atractive cost-merit and simplicity of fabrications, (2) the floating-surface N-I-P junction photodiode originally invented by Prof. Jun-ichi Nishizara in Tohoku University in 1950s [35], (3) Bell Lab 1970 invention of the CCD/MOS capacitor type buried channel photodiode with the complete charge transfer capability and the no-image-lag featur Howerever, the conductive metalic MOS electrode does not pass short-wave blue-light. And the strong surface elctric field induces undeisred surface dark current. (4) the surface-pinned completely-najority-carrier-depleted buried-channel Hole Accmutalion Photodiode (HAD) in invented by Hagiwara at Sony in October 23, 1975.

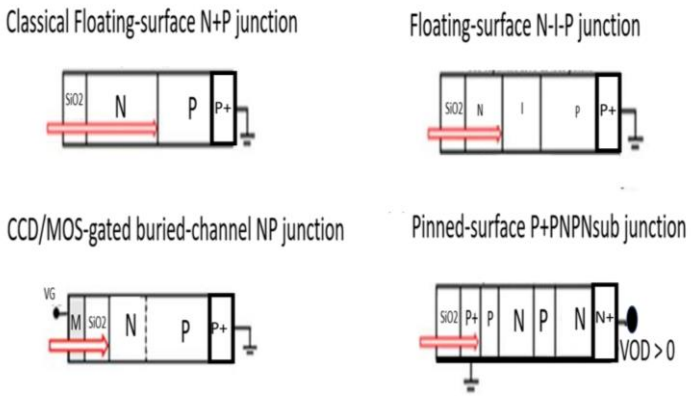

Figure 8. Various types of photo diode structures in comparison for solar cell applications.

Figure 9 shows the advantage of the newly proposed pinned-surface completely-majority-carrier-depleted buried-channel double-junction type solar cell over the conventional N+NPP+ single junction type solar cell with the smaller depletion width. The barrier potential and the strong electric field in the wide depletion region helps separating the photo electrons and holes contributing the solar cell conversion efficiency. For the single N+PP+ single junction solar cell, the depletion region is limited at most about 2 μm while the double junction P+PNPP+ solar cell can have the double-size depletion region.

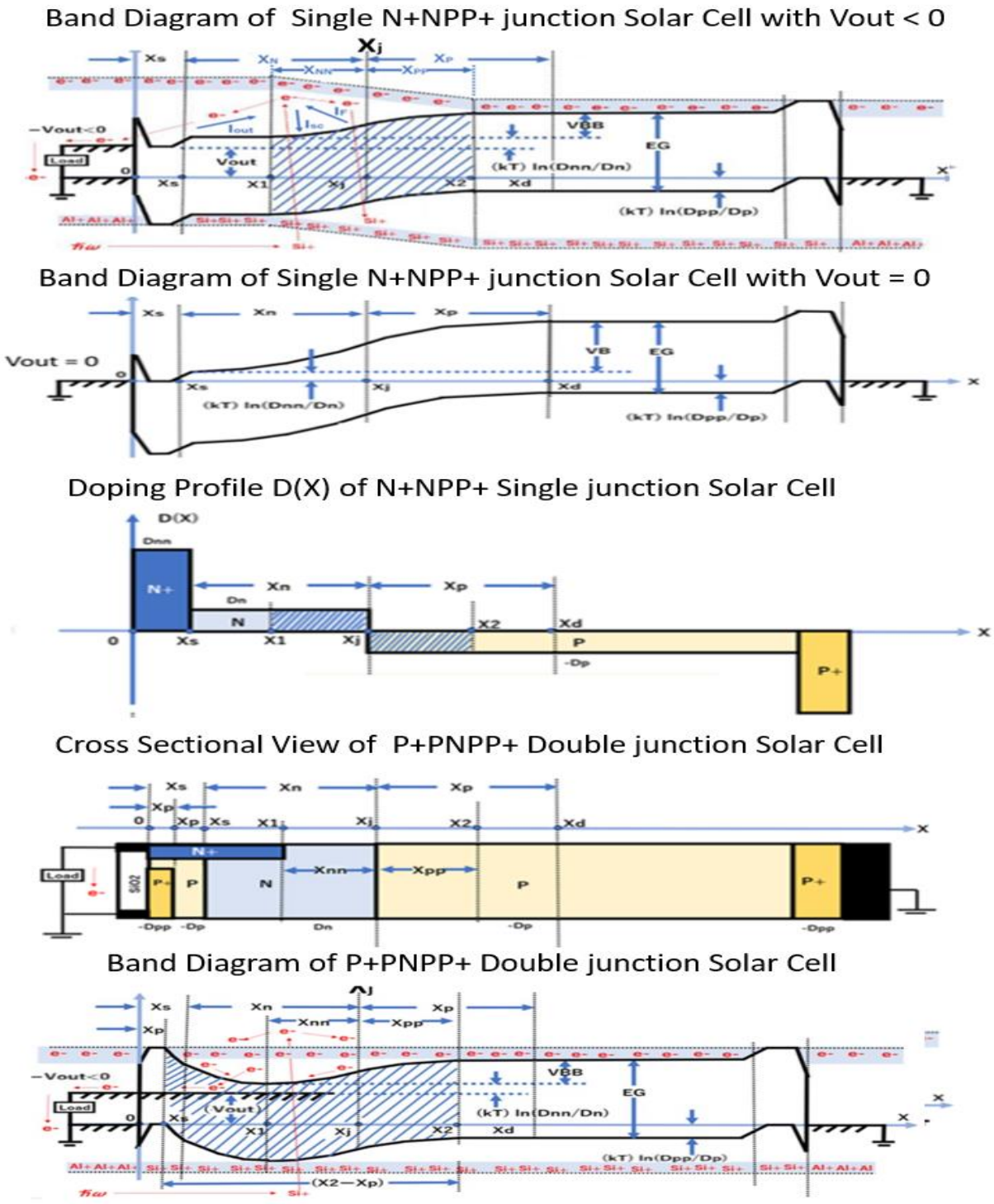

Figure 9. N+NPP+ single and P+PNPP+ double junction solar cells in comparison.

Figure 10 shows a combined structure of a small-area N+NPP+ single junction outlet photodiode and a large-area P+PNPP+ double junction photodiode with a wider depletion region for separating effectively photo elctron and hole pairs and expecting a higer photon-to-electron conversion efficiency. Figure 10a shows a floating-surface single junction solar cell with a simple standard four-mask process. Figure 10b shows a five-mask process with an additional high-energy ion implantation for the lightly-doped N region formation. Figure 10c shows a six-mask process for a pinned-surface P+PNPP+ double junction photodiode solar cell with another additional low-energy ion implantation step for forming the surface P+P region. This P+PNPP+ double junction solar cell can be applied not only for the silicon-crystal based solar cell but also for the thin-film amorphous-silicon-based solar cell and also with other base materials such as for the perovskite solar cell. The additional increase in the total production-cost is minimal since only two additional ion implantation steps for the surface P+P formation are needed.

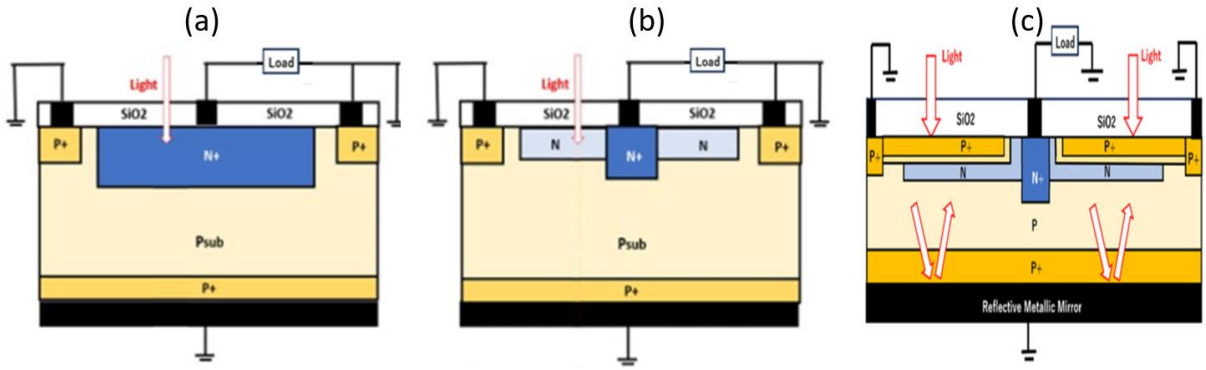

Figure 10. Two types of single junction photodiodes **(a)** and **(b)** with a double junction photodiode **(c)**.

Figure 11 explains conceptually how the large read-out bit-line capacitance is causing the undesired thermal CkT noise in classical old MOS image sensors with floating-surface single-junction photodiodes. A simple N+PsubP+ single-junction photodiode widely applied in classical MOS image sensors suffers the serious image lag problem. At the reset time, as the photo charge is being drained out of the floating-surface image sensing and storage N+ region through the charge transfer gate CTG, the potential level Vs of the photo charge sensing and storage region is slowly approaching to the level of the channel potential Vch and the difference (Vch – Vs) gets very small. The drain current Ids is governed by the relationship $Ids = Io(Vs - Vch)^2$ [36–37]. This slow draining causes the image lag.

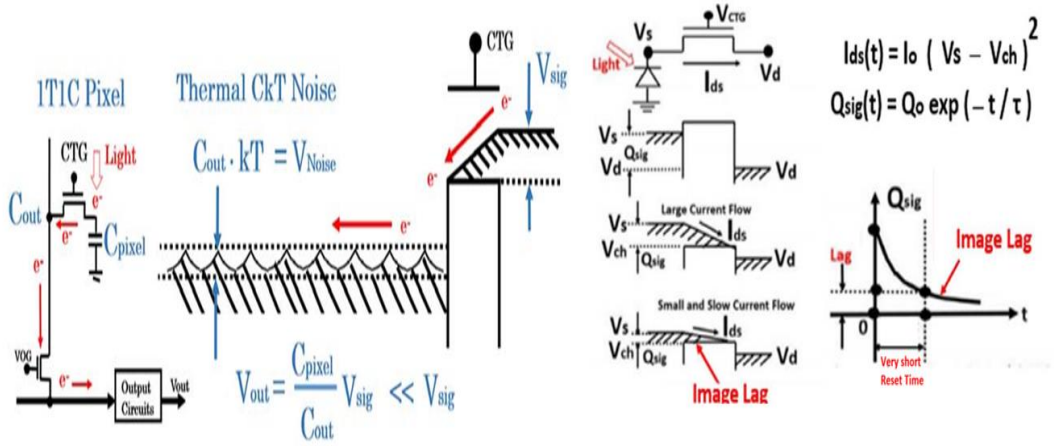

Figure 11. CkT noise and image lag in single junction photodiodes.

4. The conventional floating-surface N+NPP+ single-junction photodiode-type solar cell

Figure 12 shows a cross-sectional view of a floating-surface N+NPP+ single-junction photodiode for a solar cell application. Fermi level Ef is at the ground voltage level in P+ region while in N+ region we have $Ef = -Vout < 0$. Photo electron and hole pairs are generated in the depletion region and separated effectively by the electric field present in the depletion region. The depletion width WD can be made wider by lowering the substrate doping level DP [38].

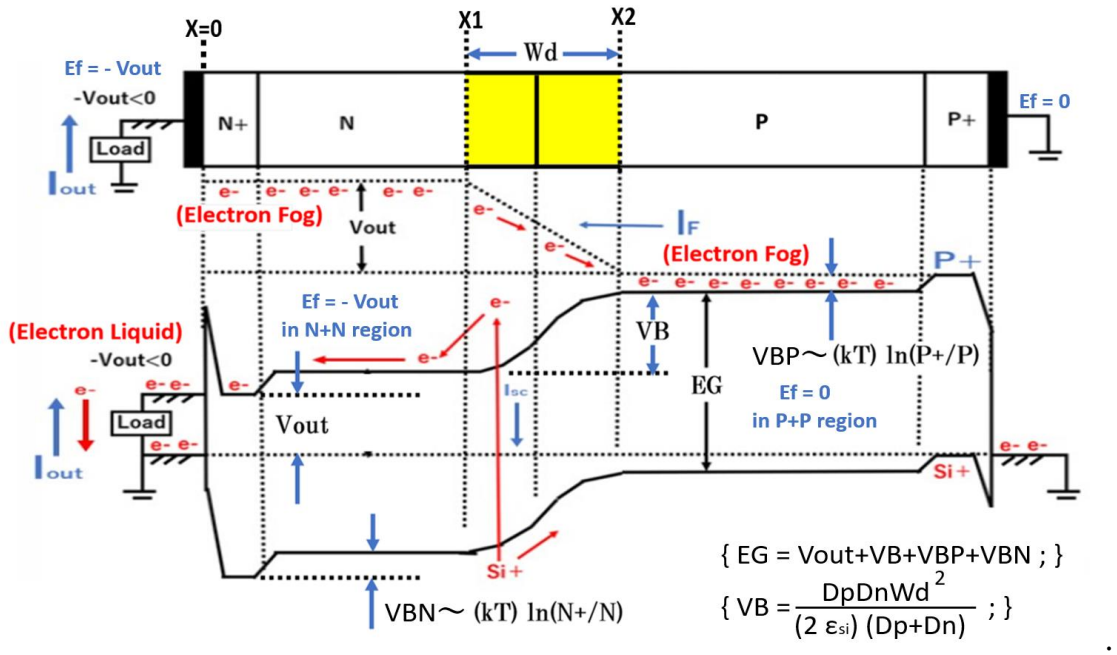

Figure 12. A floating-surface N+NPP+ single-junction photodiode for a solar cell application.

Sony developed the CCD/MOS capacitor type photo image sensors in 1980 while other competing companies used, instead, the simple floating-surface N+P singe junction type photodiode, that had some undesired demerits of the surface dark current or the image lag problems. The pinned-surface P+PNPP+ double junction photodiode invented in 1975 and developed in 1978 by Sony has a wide depletion region and also the pinned-surface P+P doping variation both work for effective separations of photo elctron and hole pairs and is expected to have a high photon-to-electron conversion efficiency.However, the backside P+ diffusion region needs to be heavily doped to form a perfect ohmic contact with the backside external metal wiring. The backside P+P doping variation gives the backside P+P barrier potential (VBP). The surface N+N type heavily doped region is needed to achieve an ohmic contact with the surface metal contact region, connecting the solar cell external output load.

The surface N+N doping variation gives the surface N+N barrier potential (VBN). We then have the relationship $EG = Vout + VB + VBN + VBP$.

The electron concentration in the N-type region is given as $n(x) = Nc\ exp\left(\left(Ec(x) - Ef\right)/kT\right)$ while the hole concentration in the P-type region is given as $p(x) = Nv\ exp\left(\left(Ef - Ev(x)\right)/kT\right)$.

The effective density Nc of the state at the edge of the conduction energy band edge Ec is given as $Nc = 1.04 \times 10^{19} cm^{-3}$ and the effective density of the state at the edge of the valence energy band as $Nv = 2.8 \times 10^{19} cm^{-3}$. We have $Ec(x) < Ef < Ev(x)$; $\rho(x) = p(x) - n(x) + D(x) = 0$ in the thermal equilibrium and the level of the Fermi level Ef can be uniquely determined accordingly.

In the P-region, we have $Ef = 0$; $Ev(x) = VBP > 0$; $Ec(x) = VBP - EG < 0$. And we get the relationship $D(x) = -DP = -Nv \exp(-VBP/kT) + Nc \exp((VBP - EG)/kT)$ while in the N-region from the relationships $Ef = -Vout$; $Ev(x) = EG - Vout - VBN > 0$; $Ec(x) = -Vout - VBN < 0$, we have the relationship $D(x) = DN = -Nv \exp((VBN - EG)/kT) + Nc \exp(-VBN/kT)$. As DN goes zero we have $VBP = (EG + kT \ln(Nv/Nc))/2$ while $VBN = (EG - kT \ln(Nv/Nc))/2$ as DN goes zero.

According to the intensity of the solar cell input photo current Isc, the output voltage Vout is controlled small, by the maximum power tracking technology (MPTT). Both substrate impurity doping DP and depletion width WD have some optimum values. In this case, when the maximum power tracking technology (MPTT) controls the output voltage Vout to be low, the VB increases, which occurs because the barrier potential VBN for the N+N junction and the barrier potential VBP for the P+P junction remain unchanged under the equation of $EG = Vout + VB + VBN + VBP$.

The solar cell input photocurrent Isc also causes a Fermi level difference across the PN junction, leading to a forward biasing of the PN junction and a decrease in the barrier potential of the PN junction VB from that of the thermal equilibrium state.

Figure 13 shows a rain-drop model of floating clouds in a clear sky over a wide-open flat ocean. Clouds are generated by the vaporized water molecules being energized by the strong sunshine in the open sky. If no wind is blowing, the clouds stay where they are born on the ocean and eventually all the rain drops fall back to the ocean again. Figure 13 also shows electron-and-hole-pair generation and recombination at the vicinity of the floating-surface N+NPP+ single junction photodiode, the movements of generation, separation and recombination of electron fog-clouds.

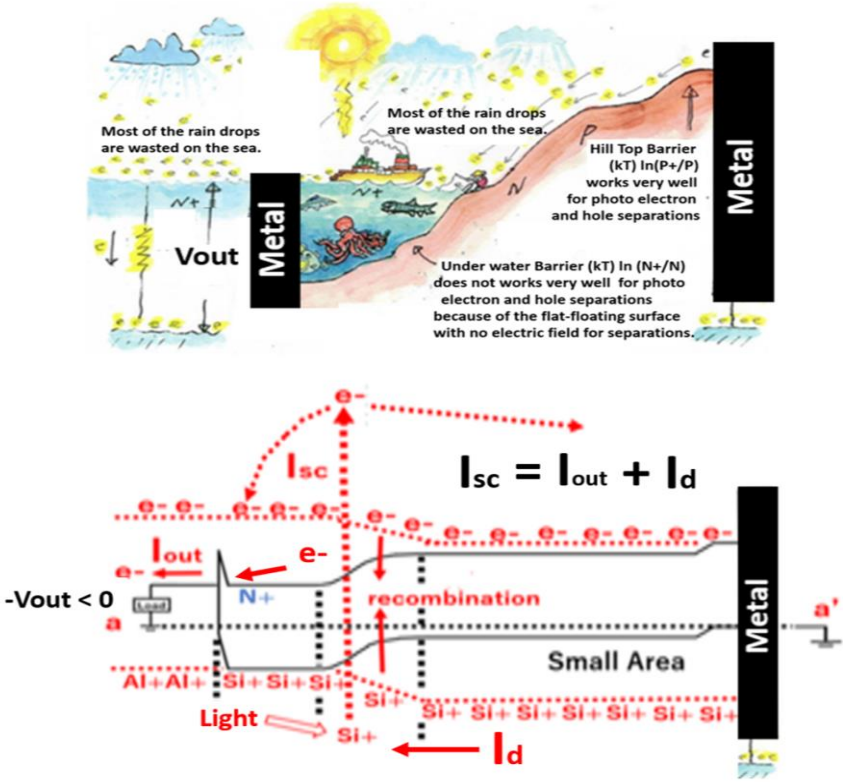

Figure 13. Photo Electron and Hole Pair Generation in N+NPP+ Single Junction Solar Cell.

Wind is a moving-force for the rainy clouds in high-energy vapor-fog state while the electric field is the moving-force for photo electron-and-hole pair separations in the depletion region of this N+NPP+ single junction type solar cell.

Only the photons reaching inside of the depletion region of the N+NP+P junction can contribute as the solar cell photo current Isc, which is the sum of the forward diode current Id and the output current Iout flowing out from the N+ outlet diffusion region. We have the relationship $Isc = Id + Iout$ with the output current Iout and the output resistance Rout $Iout = Vout / Rout$, where Vout is the solar cell output voltage and Rout is the effective solar cell output resistance.

The forward photodiode current Id is due to the high-energy vaporized hot electron fog, while the solar cell output current Iout is due to the cooled-down low-energy "liquid" electrons.

By definition, this is the reason why the solar cell power efficiency is lower than the quantum efficiency, which is defined as the ratio of the number of generated photo electrons divided by the number of illuminated photons.

Figure 14 shows a cross-sectional view of a wide-area P+PNPP+ double junction photo diode coupled with a small-area conventional N+PP+ single junction photo diode and also the band diagram of a pinned-surface P+PNPP+ double junction photodiode for a high-performance solar cell application. The cold-temperature "liquid" electrons are collected by the large-area of the middle-centered N-type completed-depleted buried-channel photo electron collector region.

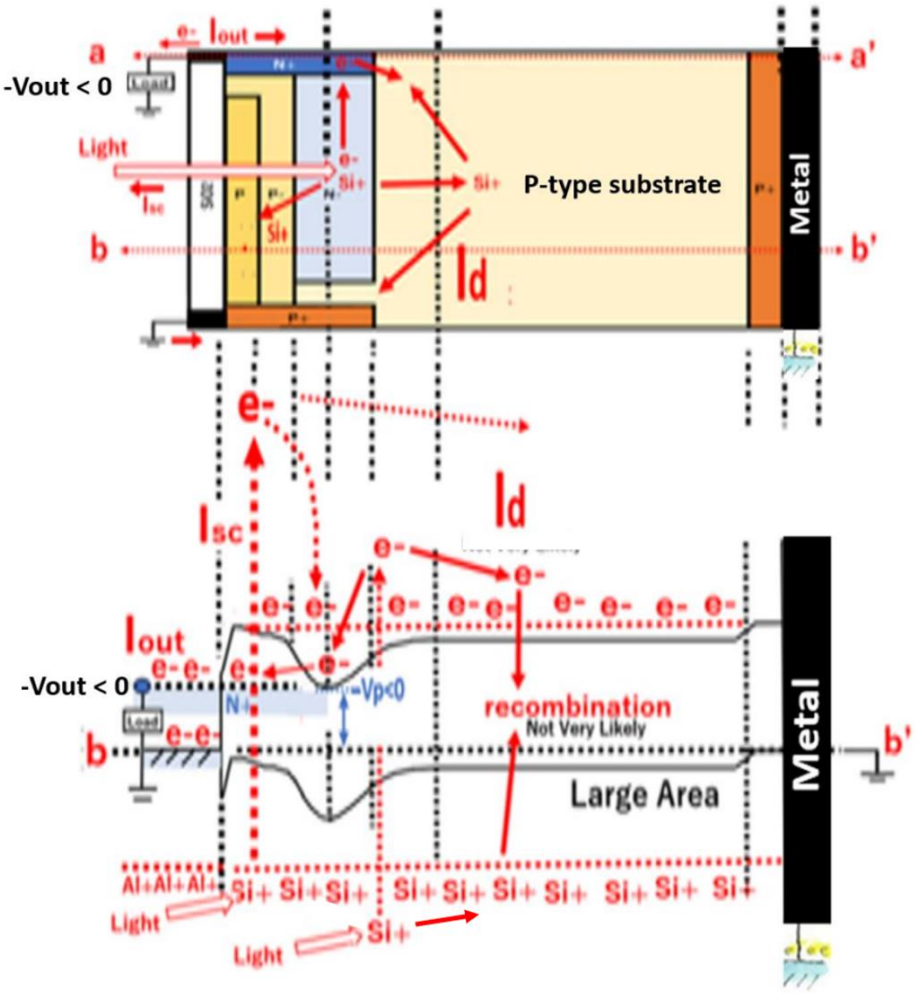

Figure 14. Photo Electron and Hole Pair Generation in P+PNPP+ Doble Junction Solar Cell.

5. P+PNPP+ double junction solar cell with pinned-surface and pinned empty-potential-well

For the visible light of the wave length $0.4\ \mu m < \lambda < 0.7\ \mu m$, silicon crystal looks very metallic dark because it does not pass the visual light with the band gap energy $EG = 1.11\ eV$, the silicon crystal is transparent for infrared light with wave-length longer than $\lambda si = 1.24 / EG = 1.12\ \mu m$. Short-wave high-energy blue light is absorbed in the vicinity of the silicon surface and wasted as heat in the conventional floating-surface N+NPP+ single junction type solar cell. For the 0.4μm range short wave-length blue-light, we need to devise a way to form the surface barrier electric field for separating the photo electron and hole pairs generated at the vicinity of the silicon crystal surface because the 0.4 μm range short wave-length blue-light cannot penetrate deep into the silicon crystal.

By the relationship $D(x) = -DP = -Nv\ \exp(-VBP / kT) + Nc\ \exp((VBP - EG) / kT)$ in the P-region, the surface conduction band bending (VBP) is created by the surface P+P impurity atom density variation, which is given approximately by $VBP \sim (kT)\ \ln(P+/P)$. This surface barrier potential (VBP) creates the surface barrier electric field for effectively separating photo electron and hole pairs generated by the short-wave light at the vicinity of the silicon crystal surface. Figure 15 shows results of numerical computations of actual electron potential profiles with the barrier height VBP created by the surface P+P impurity atom doping variation, the space charge polarization curve and a surface built-in barrier potential profile, generated by the pinned-surface P+P doping variation, by actual numerically-exact computations. The barrier potential $VBP = (kT)\ \ln(P+/P)$, created by the P+P doping variation, was found to be extending from the silicon surface $X = 0$ to more than 1 μm depth in silicon $X > 1\ \mu m$, wide enough to separate photo electrons and hole pairs at the pinned-surface P+P region. Since there is no silicon chip yet, which is under preparations, no real data is available for comparison between the conventional and the proposed double-junction solar cells. Expected results will be published as soon as the silicon chip is fabricated.

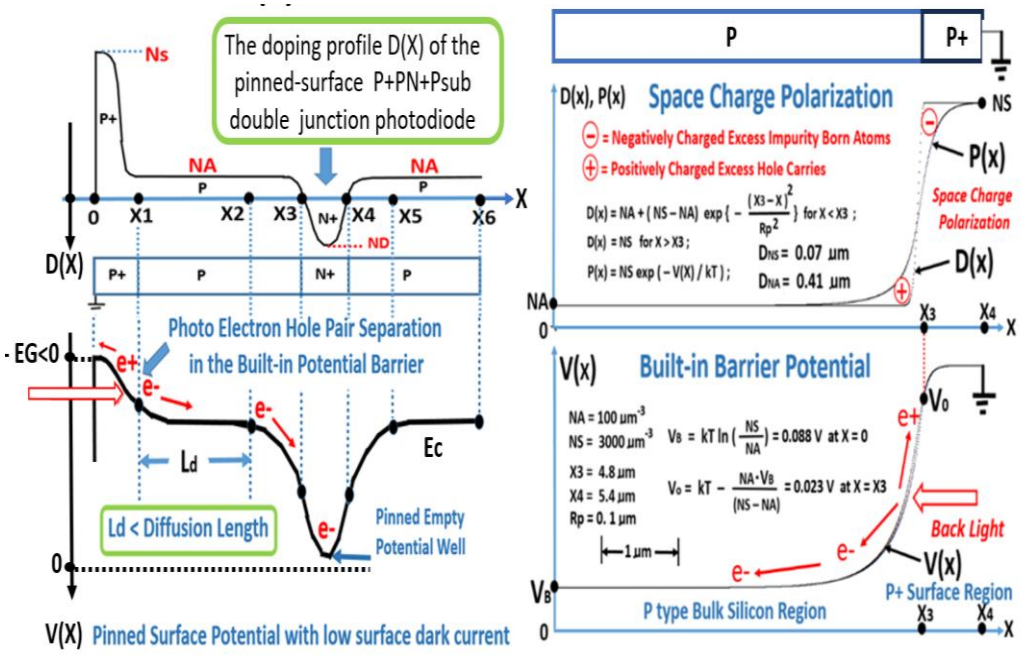

Figure 15. Pinned Surface P+P Potential Barrier Profile and its space chare polarization profile.

Figure 16 shows two types of configurations for double junction solar cells. The P+PNPP+ double junction photodiode shown on the left in Figure 16 has the P+PNPP+ doping profile, which is symmetric at the middle-point, centered by the buried-channel N region with a symmetric pinned empty potential well. Hence, we expect a wider and doubled depletion width $Wd = [X1, X2]$ for the pinned-surface P+PNPP+ double junction pinned photo diode. The pinned-surface P+ hole accumulation regions both in the surface and the backside create the surface P+P barrier potential $VBP \sim kT \ \ln(P+/P)$ for $Nv \sim P+ < P$, which gives $VBP \to EG/2$ as the substrate doping DP gets very low, as governed by the relationship $DP = Nv \ \exp(-VBP/kT) - Nc \ \exp((VBP - EG)/kT)$.

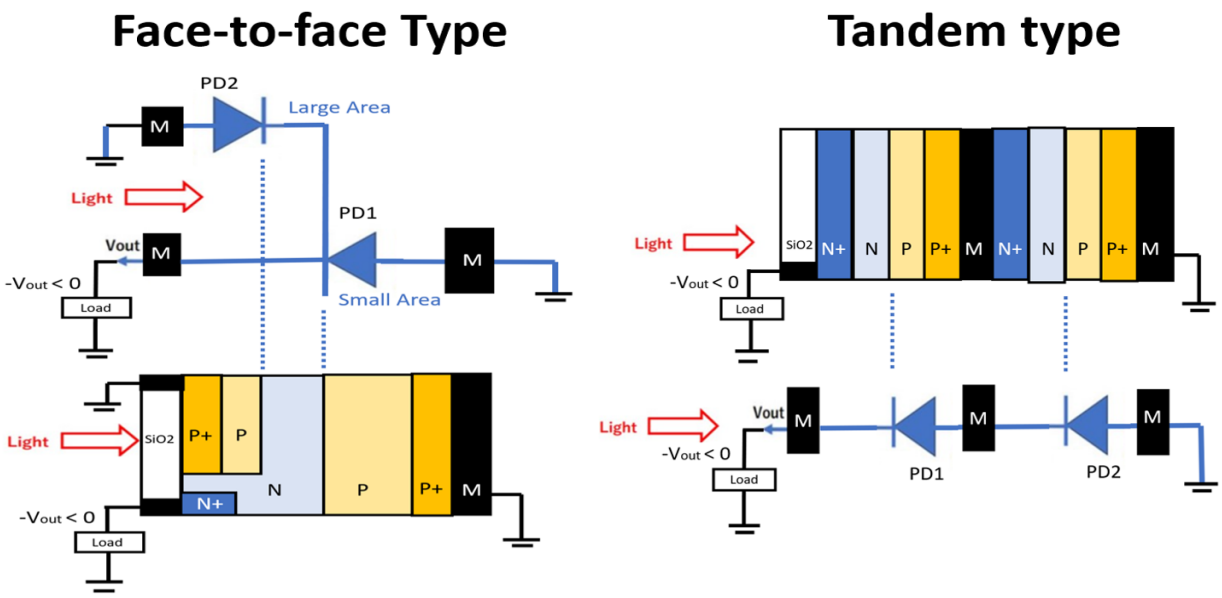

Figure 16. Two types of Double Junction Solar Cells in comparison.

Both at the surface and the backside P+P impurity doping variations give a barrier potential VBP, separating effectively the minority carrier photo electron and hole pairs in the P+P pinned-surface heavily-doped hole-accumulation regions while majority carrier holes both at the front surface region and the back surface region see only the flat sea of hole majority carriers with no moving force.

Figure 16 on the right shows two N+NPP+ single photodiodes connected with a metallic ohmic contact region in-between in tandem formation [39–40]. The structure looks very complex and costly with the extra metallic region in-between. The N+NPP+ single junction type solar cell is a simple, low-cost and very attractive. However, the double-junction tandem solar cell needs an undesired metallic ohmic bridging-layer in-between. For the triple junction tandem solar cell, we need two extra undesired metallic ohmic bridging-layers in-between. Thin film amorphous silicon and Perovskite solar cells are considered more attractive cost-wise instead of the silicon crystal type solar cells.

In order to have good ohmic contacts with the undesired metallic bridging-layers, for each N+NPP+ single junction photodiode, the heavily doped N+ and P+ regions are needed. However, the P+P and N+N variation induced barrier potentials VBP and VBN both decrease the magnitude of the output voltage Vout since we have $Vout = EG - VB - VBP - VBN$. A single PN junction depletion width (Wd) is computed by the relationship $VB = Wd^2 \times DP / (2\varepsilon_{si})$ and $Wd = sqrt(2\varepsilon_{si} VB / DP)$. The width (WD) of the depletion region needs to be kept wide enough for effectively separations of the photo electron and hole pairs in the NP junction depletion region in order to achieve a good solar cell efficiency.

However, these barrier potentials VBP and VBN give the undesired effects of minimizing the output voltage Vout, which is governed by the relationship $Vout = EG - VB - VBN - VBP > 0$. Using the depletion width Wd as an independent variable and the p-type substrate doping level DP as another independent parameter, we can now compute the values of the solar cell output voltage Vout, using the relationship $Vout = EG - VB - VBN - VBP > 0$.

Figure 17 shows the values of the output voltage Vout, which is computed and plotted along the Y-axis, as a function of the depletion width Wd, taken along the X-axis, with an independent parameter of the substrate doping level DP. Two extreme cases with values $DP = 1\ \mu m^{-3}$ and $DP = 1000\ \mu m^{-3}$ are shown in the simplified case with the condition $D(X) = DN \to N+$. The output voltage Vout is found to be centered around $Vout \sim 0.4\ volt$, and we have $0.7\mu m < Wd < 2.4\ \mu m$.

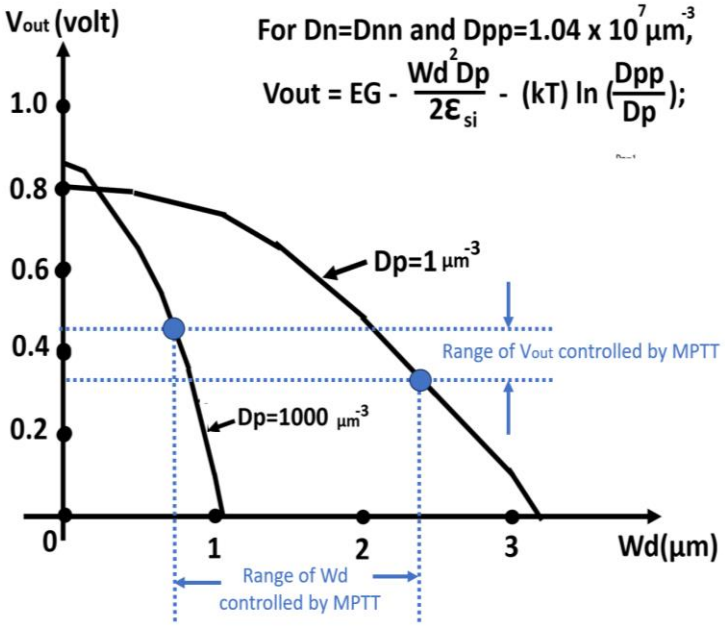

Figure 17. Expected Output Voltage Vout of Floating-Surface N+PP+ Single Junction Solar Cell.

6. The conditions to obtain the maximum power in the N+NPP+ single-junction photodiode

The total internal solar cell photo current Isc is generated according to the intensity of the illuminated sun light. For the case of a floating-surface N+NPP+ single-junction type photo diode, we have the relationship (1) $Isc = Iout + Id$. The output current Iout and the forward-biased current Id shares the solar cell current Isc. However, for the case of the pinned-surface P+PNPP+ double junction, we have another surface-side photodiode current Ids which also shares the solar cell photo current Isc. And we have the relationship (1a) $Isc = Iout + Id + Ids$. The output power of the solar cell is simply given as the product $Power = (Iout)(Vout)$.

The photodiode forward current Id is given as (2) $Id = Io\left(exp(Vout + Vs)/kT\right) - 1$ where the constant $Io = Ao\ exp(-EG/kT)$ is depending on the size (Ao) of solar cell photodiode. The N+NPP+ single-junction photodiode with the output voltage of $(-Vout) < 0$ becomes forward biased as the intensity of the sun light illumination increases. We also have the relationship between the substrate resistance Rs and the undesired voltage drop Vs as (3) $Vs = Rs \times Id > 0$.

The optimum value of the effective output resistance Rout is controlled for the maximum solar cell power point, by the maximum power tracking technology (MPTT) [41–43]. The output current Iout and the output voltage are related as (4) $Vout = Iout \times Rout$; or $Rout = Vout / Iout$. Since the solar cell power is defined as (A) $Power = (Vout)(Iout)$ and for the maximum power point, by solving the differential equation (B) $d(Power)/d(Vout) = 0$, we obtain the output current as (5) $(Iout/Isc) = (Vout/kT)(1+Rs/Rout)/\left(1+(Vout/kT)(1+Rs/Rout) - exp\left(-(Vs + Vout)/kT\right)\right)$.

Figure 18 shows a computational flow chart to get the output current Isc. From the relationship (5), then for the simple case of the zero-substrate resistance $Rs = 0$, we have the output current Iout/Isc as (6) $(Iout/Isc) = (Vout/kT)/\left(1+(Vout/kT) - exp(-Vout)/kT\right)$. See Figure 19.

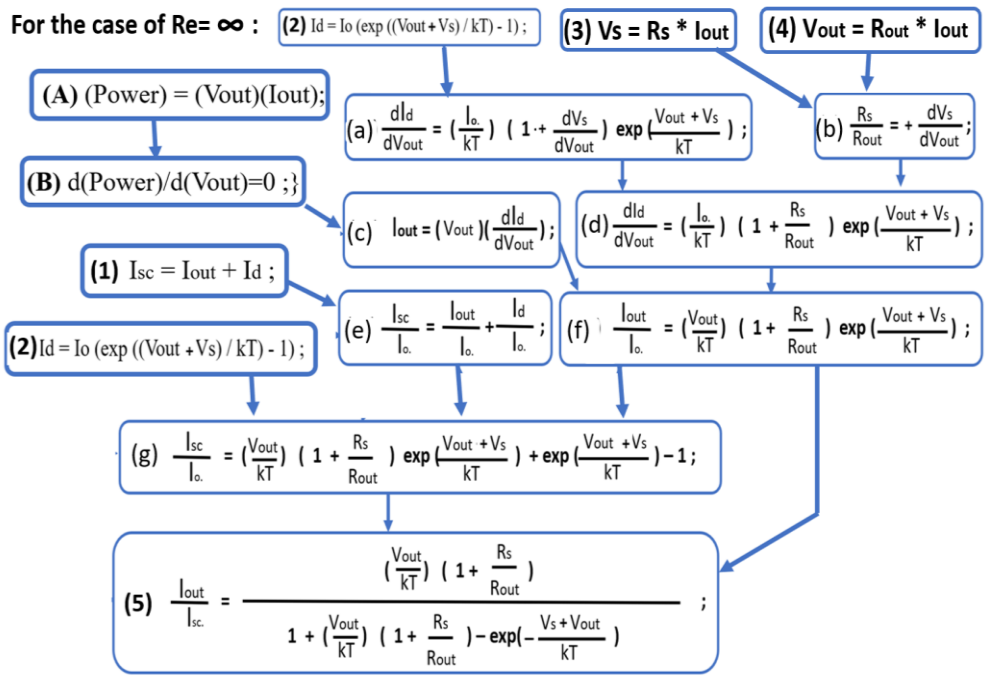

Figure 18. A flow chart of a salient computational algorithm to obtain the value of (Iout/Isc).

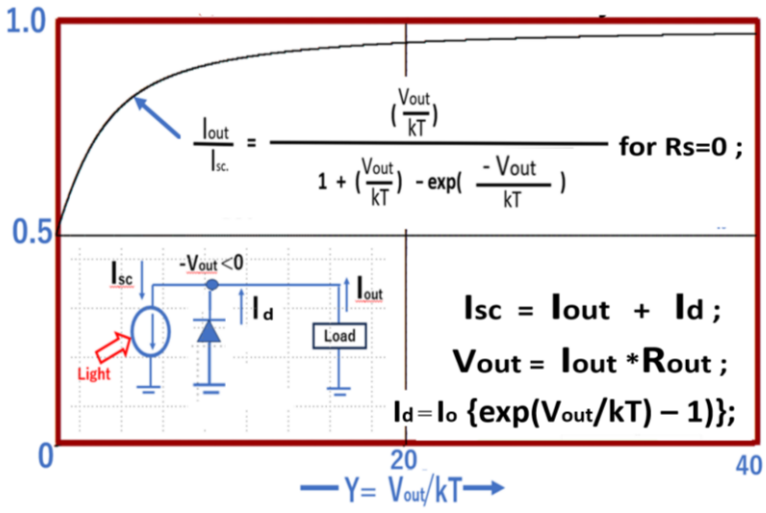

Figure 19. The dependence of the output current Iout upon Vout for the case of Rs=0.

7. The dependence of the solar cell output power upon the substrate resistance Rs

For the special ideal case of the zero-substrate resistance $Rs = 0$, the value of Iout/Isc changes from 50% to 100% while the output voltage Vout/kT increases from zero to $EG / kT = 42.9$ where we have the values of the silicon band gap energy $EG = 1.11\ eV$ and the thermal energy $kT = 0.0259\ eV$.

The solar cell photodiode (Isc/Io) and the substrate resistance Rs are the two external independent parameters. The value of the solar cell output current Iout/Isc is controlled fairly well with a very small variation in the range between 50% and 100% as shown in Figure 20 on the left.

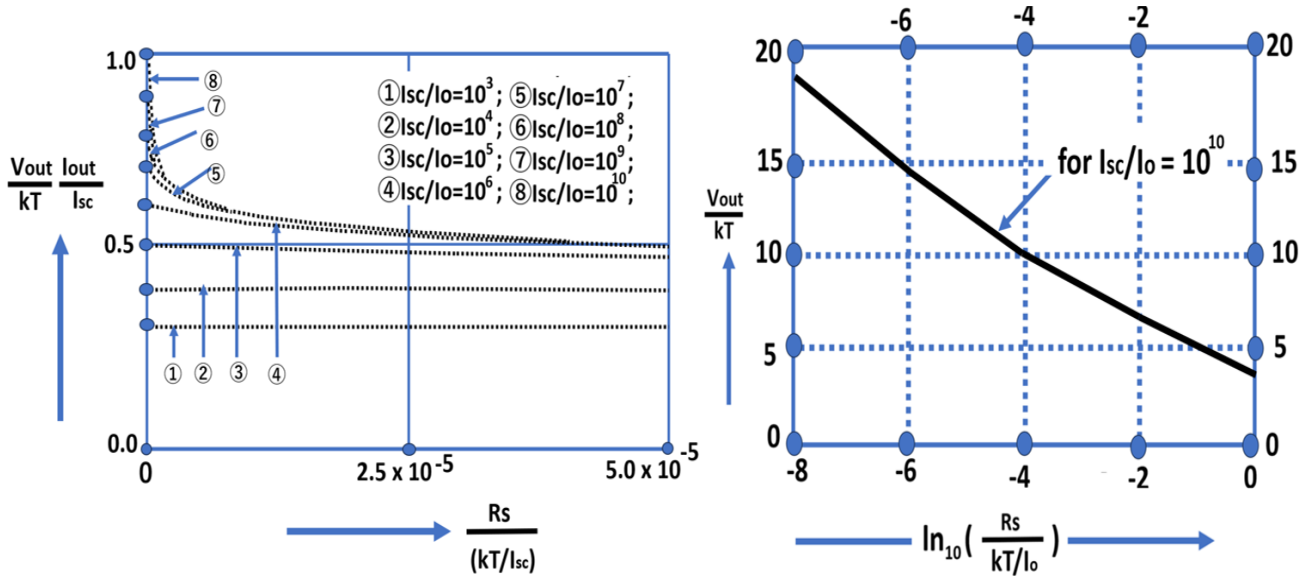

Figure 20. The dependence of the power and the output voltage upon the substrate resistance Rs.

Three parameters, (Iout/Isc), (Vout/kT)(Iout/Isc) and (Vout/kT) / (Iout/Isc), are physical parameters normalized by the solar cell photo current Isc and the thermal energy kT. Their values are well controlled and do not change much.

Figure 20 on the right shows the dependence of the output voltage Vout/kT upon the magnitude of the normalized substrate resistance Rs × Io/kT. The magnitude of the substrate resistance Rs has a strong undesired effect of decreasing the output voltage Vout/kT significantly. The DC-to-DC converter technology is widely applied to raise the solar cell output voltage Vout. The small value of the solar cell output voltage Vout is not very much welcomed in practice.

The substrate resistance Rs and the solar cell photo current Isc are two independent uncontrollable parameters. By a wise scheme of Maximum Power Tracking Technology (MPTT), the output resistance Rout and the low output voltage Vout are controlled at a fairly-controlled low level.

With the five basic relationships governing the solar cell performance, as explained below, the values of the five basic important physical parameters Id, Vs, Rout, Vout and Iout, are uniquely determined numerically from the values of the two independent input physical parameters Rs and Isc.

There are the same number of the governing Equations (1) through (5) shown below with the five unknown parameters Id, Vs, Rout, Vout and Iout.

The computational algorithm is as followed: As a first guess, set the value of the solar cell output current as $Iout = Isc / 2$. Then follow the steps shown below and repeat the iteration till conversion.

Step (1): get Id from (1) $Isc = Iout + Id$. Step (2): get Vs From (3) $Vs = Rs \times Id$. Step (3): get the value of Vout from (2) $Id = Io\left(exp\left(\left(Vout - Vs\right) / kT\right) - 1\right)$. Step (4): get the value of Rout form (4) $Vout = Iout \times Rout$. Then we get a new value of the output current Iout from the next step defined as Step (5): $\left(Iout / Isc\right) = \left(Vout / kT\right)\left(1 + Rs / Rout\right) / \left(1 + \left(Vout / kT\right)\left(1 + Rs / Rout\right) - exp\left(\left(Vs - Vout\right) / kT\right)\right)$.

And then return to the Step (1) until we get the final exact values Id, Vs, Rout and Iout. By repeating the iteration steps $(1) \rightarrow (3) \rightarrow (2) \rightarrow (4) \rightarrow (5) \rightarrow (1)$ sufficient times, we get the final values of the five unknown parameters Id, Vs, Rout and Iout as shown in Figure 19 and Figure 20 above.

8. Photon-to-electron conversion efficiency of the single junction type solar cell

Figure 21 shows another possible future solar cell application of a multi-junction Face-to-Face type pinned-surface and buried-channel type photodiode with the pinned-surface P+P doping variation and the fully-depleted buried N− regions. A very high-resistivity silicon crystal makes a large joule-heat power loss although the substrate is pinned by the heavily doped backside P+ region with a perfect direct ohmic contact with the external metal wiring in the backside. This structure is suited for multi-junction thin-film solar cells such as amorphous-silicon and perovskite types. This multi-junction Face-to-Face pinned-surface hole-accumulation photodiode (HAD) type solar cell has a very high quantum-efficiency (QE) expectation.

There are three statistical distribution functions, (1) the Maxwell-Boltzmann statistics for identical and distinguishable particles, (2) Bose-Einstein for identical and indistinguishable particles that do not obey exclusive principle and (3) Fermi-Dirac for identical and distinguishable particles that obey the exclusion principle [44].

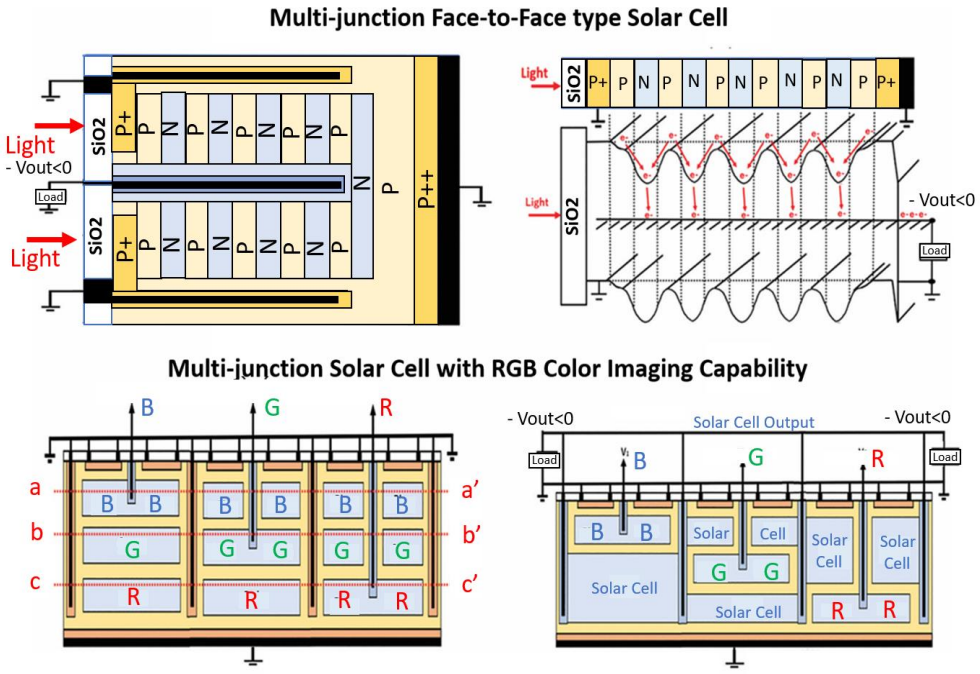

Figure 21. P+PNPN~PNPP+ multi-junction multi-layer face-to-face type solar cell.

Figure 22a shows the widely-known measured data of the sun light power density spectrum S(λ) at the sea level as a function of the wave length (λ) of the illuminated sun light along the X-axis. Figure 22b

shows the photon number density N(λ) of the sun light illuminated at the sea level, which is computed from the sun light power density spectrum S(λ) by the relationship $S(\lambda)=(hf)\,N(\lambda)$ and using the basic relationships $\lambda(\mu\mathrm{m})=hc/EG(eV)=1.24/EG(eV)$; $c=f\lambda$; $hf=hc/\lambda$.

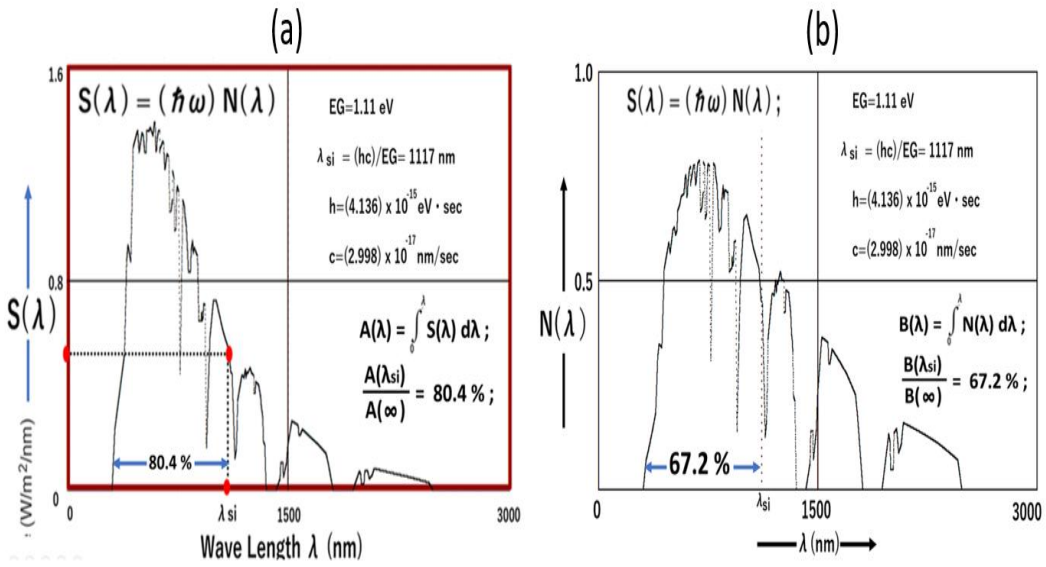

Figure 22. (a) Sun-light power density S(λ) and **(b)** the photon number density N(λ).

In 1960s, these data were not available and Shockley used this black body radiation model and considered the sun as a black body [45–47]. Shockley used a black body radiation model and considered the sun as a black body of the 6000 Kelvin, which gives the thermal energy of $kT=0.517\ eV$.

He reported the theoretical upper limit 43% of the quantum efficiency (QE), the percentage (%) of the conversion ratio of the photon number to the electron number in a floating-surface N+P single junction type solar cell. See Figure 23a. Now accurate experimental data are available and Figure 23b shows the actual quantum efficiency as a function of the photon wave length (λ) using the actual measured data of the sunlight power spectrum density without the back-body radiation model.

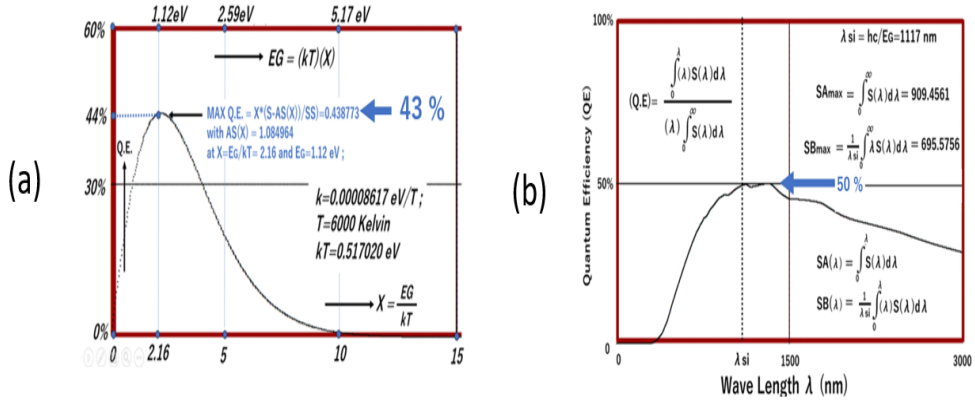

Figure 23. Energy efficiency **(a)** by black body radiation model and **(b)** by actual measurement.

In the classical black-black body radiation model, a photon gas in a cavity also behaves as electro-magnetic waves like the harmonic oscillators in the cavity, which is subject to Bose-Einstein statistics. For photon gas, the Bose-Einstein distribution function $F_{BE}(f)$ is applicable. The frequency f is related by the speed of light c as $c = f\lambda$. A photon gas in a cavity is governed by the relationship $F_{BE}(f)df = 8\pi hf^3 df / \left(exp(hf/kT) - 1\right)$. Only photons with the energy greater than the silicon band gap energy of $EG = 1.11\,eV$ can contribute to the photon-to-electron energy conversion efficiency. The percentage (%) of the illuminated light with the photon energy density S(λ) decreases drastically for the short-wave blue-light photon of the wave length less than about $\lambda = 0.4\ \mu m$, in both cases of the classical black-black body radiation model and the actual measured spectrum power model.

9. Percentage (%) of photon numbers penetrating the silicon crystal of arbitrary thickness

For photons with a long wave length λmore than $\lambda = 1.117\ \mu m = 1.24/(1.11eV)$, the silicon crystal is transparent. The entire depletion region $Wd = [X1, X2]$ becomes a transparent region for a photon with a long wave length longer than $\lambda = 1.117\ \mu m$.

About $T_1 = 95\%$ of photons with wave length greater than $\lambda_1 = 0.8\ \mu m$ are known to pass through the silicon crystal of thickness $X_1 = 0.56\ \mu m$ while about $T_1 = 37\%$ of photons with the wave length greater than $\lambda_1 = 0.5\ \mu m$ are known to pass through the silicon crystal of thickness $X_1 = 0.56\ \mu m$ [48].

With the two points data at wave length $\lambda_1 = 0.8\ \mu m$ and $\lambda_1 = 0.5\ \mu m$, as shown in Figure 24 on the left, any percentage $T_\lambda(X)$ of the photon number passing through at any depth X(μm) can be now estimated for any wave length λ(μm) for the wide range of λ= 0.4 μm and 1.1 μm.

From the two-point measured data, the values of the unknown parameters a and b for the function $A(\lambda) = a\lambda^b$ can be estimated. Then values of the model function $T_\lambda(X) = exp(-X/A(\lambda))$ can be computed for the cases of λ= 0.4μm, 0.7μm and 1.1μm as shown in Figure 24 on the right.

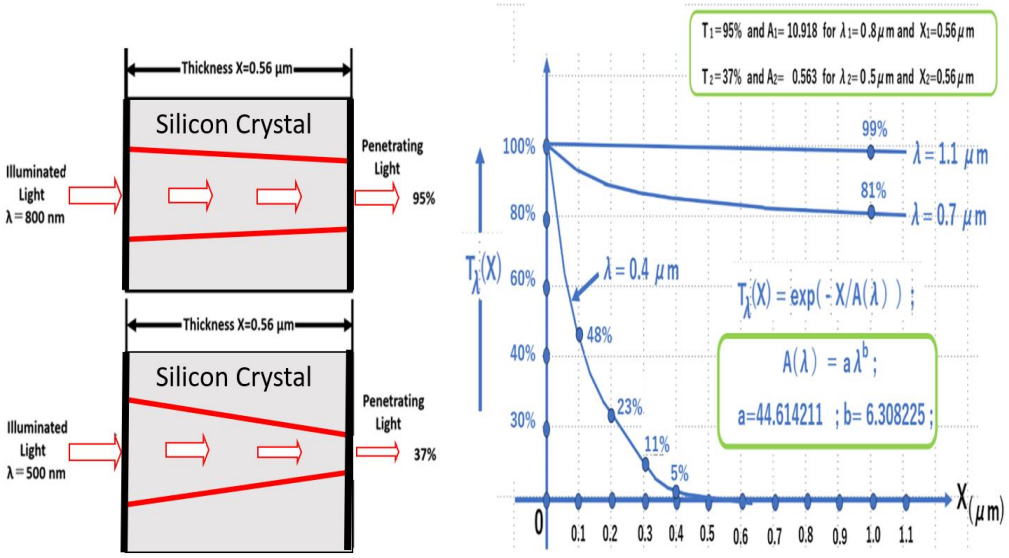

Figure 24. Percentage (%) of photons penetrating in the depth X(μm) in silicon crystal.

The sun-light power spectrum $Y_x(\lambda) = S(\lambda)\ exp\left(-X / A(\lambda)\right)$ is computed as a function of the photon wave length λ with the silicon-crystal depth X as a parameter. Figure 25a is for the silicon crystal depth X = 0.1 μm and 0.2 μm. And Figure 25b is for the silicon crystal depth X = 0.5 μm and 1.0 μm.

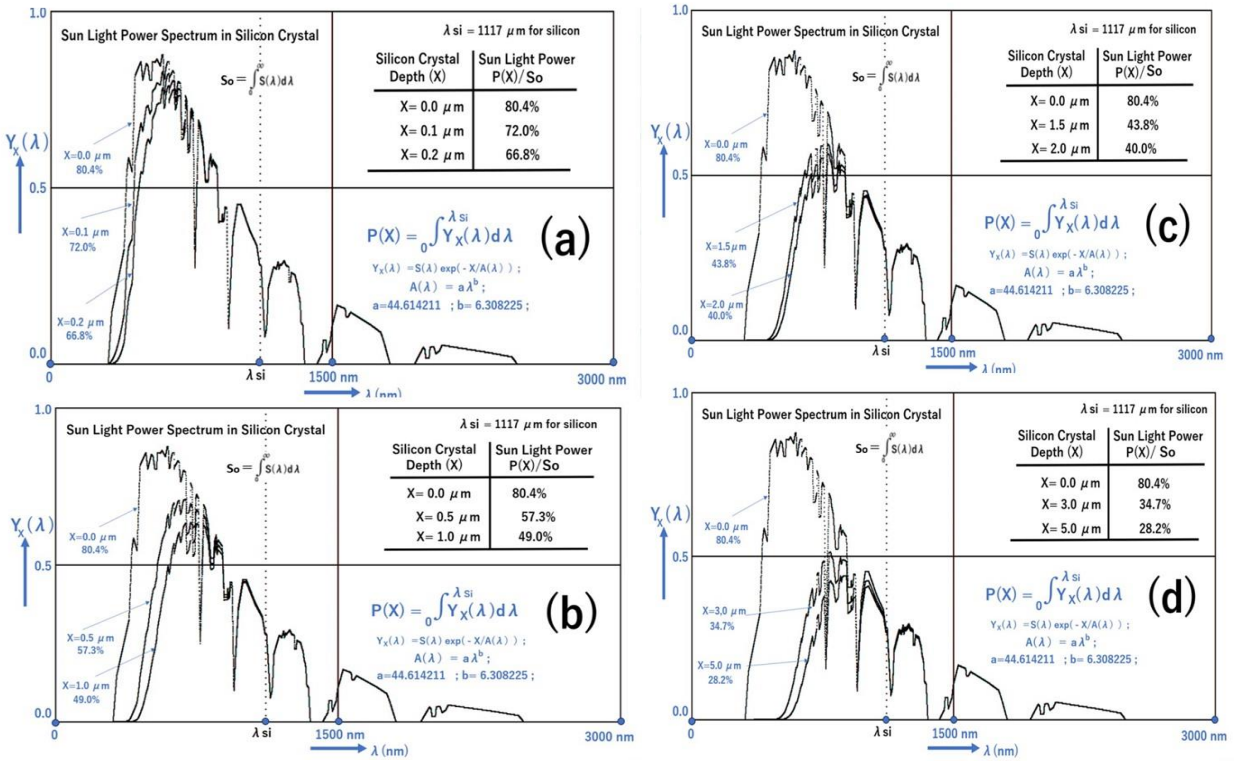

Figure 25. (a), **(b)**, **(c)** and **(d)** Sun-light Power Spectrum penetrating at the silicon crystal depth X.

Figure 25c is for the silicon crystal depth X = 1.5 μm and 2.0 μm. And Figure 25d is for the silicon crystal depth X = 3.0 μm and 5.0 μm. Note that within the 5.0 μm depth from the silicon surface, about the half (80.4 − 28.2) = 52.2% of the short-wave high-energy photons are absorbed and wasted as heat loss.

10. Percentage (%) of sun-light power penetrating through silicon crystal depth X(μm)

For a very high resistivity P-type silicon of about 100ohm cm, the depletion width WD of a single PN junction type Solar cell is known, by a simple calculation, to be about 2.2 μm for the forward-biased solar cell output voltage of Vout = 0.3 volt. For photons with the energy less than the silicon band gap energy of 1.1 eV, the semiconductor material itself looks transparent and the photons pass through the semiconductor material of any substrate thickness.

Only 80.3% of the sun light power illuminated at the silicon surface X = 0 is absorbed theoretically into the silicon crystal and become heat or useful electron energy. The remaining 19.6% of the illuminated sun light photons have the energy less than the silicon crystal band gap energy, and the silicon crystal looks completely transparent. S(λ) is the sun-light power spectrum at the silicon surface.

Penetrating through the silicon crystal, the sun-light power spectrum decreases at the silicon crystal depth X with the factor $T_\lambda(X) = exp\left(-X/A(\lambda)\right)$ with $A(\lambda) = a\lambda^b$. Figure 26 shows the dependence of the total sun-light power as a function of the silicon crystal depth (X) obtained using the results shown

in Figure 25. Sunlight power percentage$\varepsilon(X)$, penetrating the silicon crystal at the silicon crystal depth X, can be computed by integrating the product given as $S(\lambda)\,T_\lambda(X)$ for $\lambda = 0$ to $\lambda = \infty$.

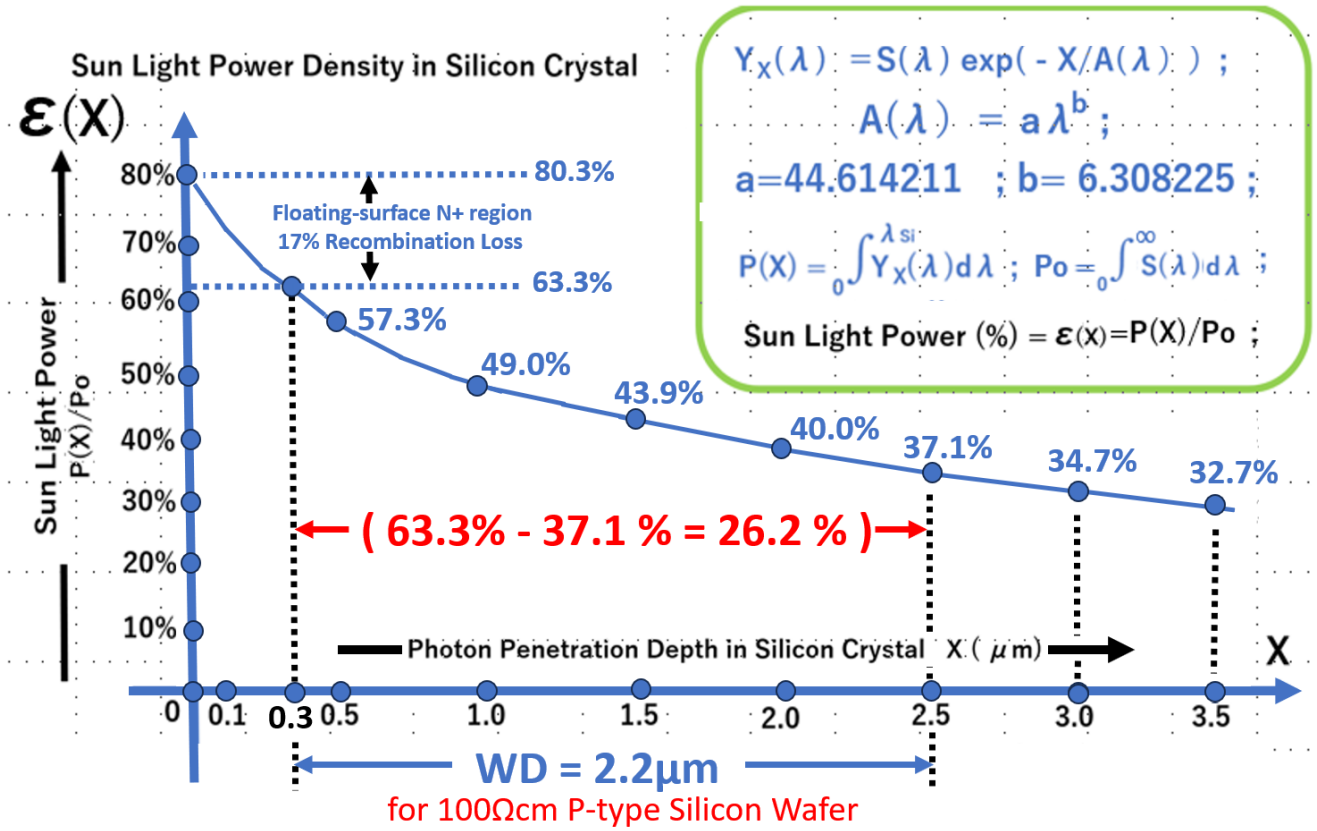

Figure 26. Sun-light power percentage$\varepsilon(X)$ penetrating through silicon crystal at the depth X.

The curve shown in Figure 26 explains, in case of the floating-surface single-junction N+NPP+ junction type photodiode, we have a depletion width $Wd = [X1, X2] = [0.2, 2.0]$ and the efficiency is only 66.8 − 40.0 = 26.8%. The electronic potential in the floating-surface N+ region $[0, X1] = [0.0, 0.2]$ is flat with no electric field for photo electron and hole separations. And the pairs are recombined and wasted as heat. In case of the pinned-surface P+PNPP+ double junction photodiode, the pinned-surface P+P doping variation gives the surface barrier potential of kT ln(P+/P), which creates the surface barrier electric field, enhancing the photo electron and hole effective pair separations at the surface.

For $X1 = 0$ and $X2 = 2.0\ \mu m$ the depletion width $Wd = [0.0, 2.0]$ gives 40.4% efficiency. By high-energy ion implantation technology, for the depletion depth of $X2 = 3.5\ \mu m$, the solar cell efficiency of $80.4 - 32.7 = 47.7\%$ is expected for this Sony HAD sensor type solar cell. If we can realize an extremely wide and maximum depletion width with $X2 > 5.0\ \mu m$ in a multi-junction such as a P+PN-PN-P+ triple junction silicon-based solar cell by our future advance technology, we would expect to have a solar cell efficiency close to the limiting value of 80.4%.

11. Maximum Power Tracking Technology (MPTT) to extract Maximum Solar Cell Power

The governing relationships are given as $Vout = EG - BV - BVn - BVp > 0$ with the barrier potential VB given as $VB = Wd^2 \times Dp / (2\varepsilon_{si})$ for the N+NPP+ single junction photodiode with the floating-surface N+N doping-variation-induced barrier potential given as $VBn = (kT)\ ln\ (Dnn / Dn)$ and the heavily-

doped-substrate ohmic-contact P+P doping-variation induced one as $VBp = (kT)\ ln(Dpp / Dp)$. The solar cell output voltage Vout is controlled by the maximum power tracking technology (MPTT) scheme according to the intensity of the illuminated sun light, which determines the solar cell output current Isc as an independent parameter. See Figure 27.

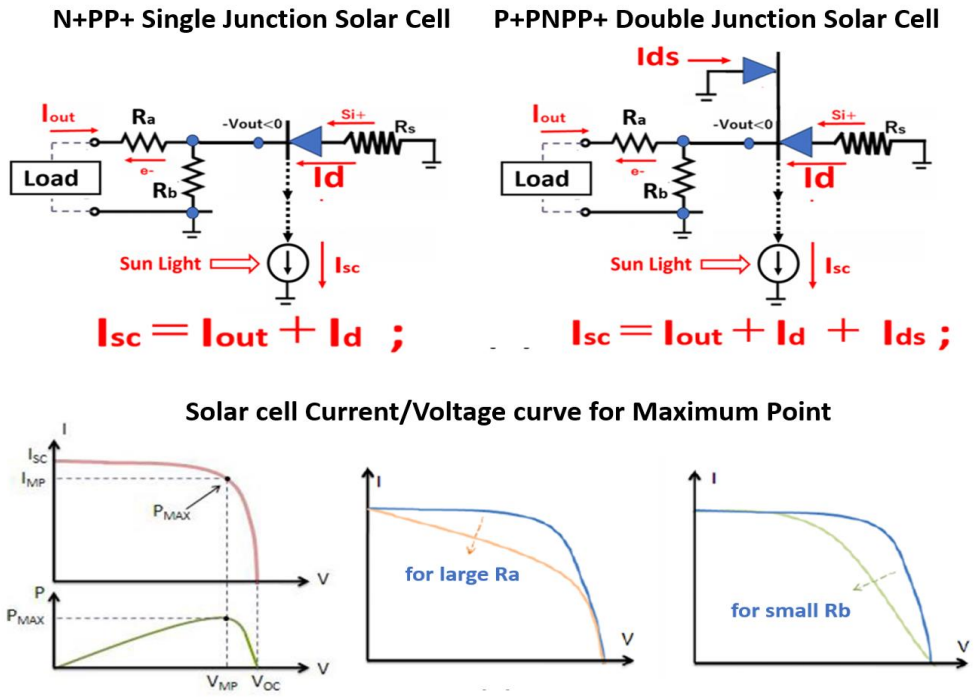

Figure 27. The MPTT scheme applied both for the single and double junction type solar cells.

The external MPTT control system optimizes the output voltage by keeping the PN junction depletion width Wd at an optimum value for the effective photo electron and hole pair separations in order to achieve the maximum power $Power = (Vout)(Iout)$ for the solar cell. By calculating the equation given by relationship $d(Power)/d(Vout) = 0$, we obtain the optimum values of Vout and Iout and then the value of the load resistance $Rout = Vout / Iout$ [49–50].

By changing the values of the resistance Ra and Rb according to the intensity of the sun light, we can adjust the output current Iout and optimize the values of the output voltage Vout and the output resistance Rout for maximum power output. The photo current $Isc = Iout + Id$ is the sum of the small-area output current Iout and the large-area forward photodiode currents Id. The internal photo current Isc is given as $Isc = Iout + Id + Ids$ for the double junction photodiode shown, which is the sum of the output current Iout and the two forward-biased currents (Id + Ids), one as the Id current for a small-area photodiode and the other one as the Ids current for a large-area photodiode.

12. Artificial Intelligent Partner System (AIPS) supported by high-performance image sensors

In analogy of behaviors of water molecules directed and collected in an underground small-area water storage beneath the large-area, dry and always-empty water-dam, the photo electron charge carriers (electron and hole pairs) behave similarly in the pinned-surface P+PNPP+ double junction photodiode type solar cell structure. The beach wave-front barrier model for a diode and the water-gate model for a switching transistor are well known and well accepted. The concept of the artificial intelligent partner

system (AIPS) is explained in Figure 28, which used originally in 2008 Sony Play Station III Cell Processors together with a large number of video cameras to realize a real-time fast-action friendly assistant and care system, supported by the wire-less real-time communication network. Many semiconductor device elements are needed.

The concept of the video assistant referee (VAR) [51–54], now applied and used worldwide, is very similar to the original concept of the Artificial Intelligent Partner System (AIPS) introduced in 2008.

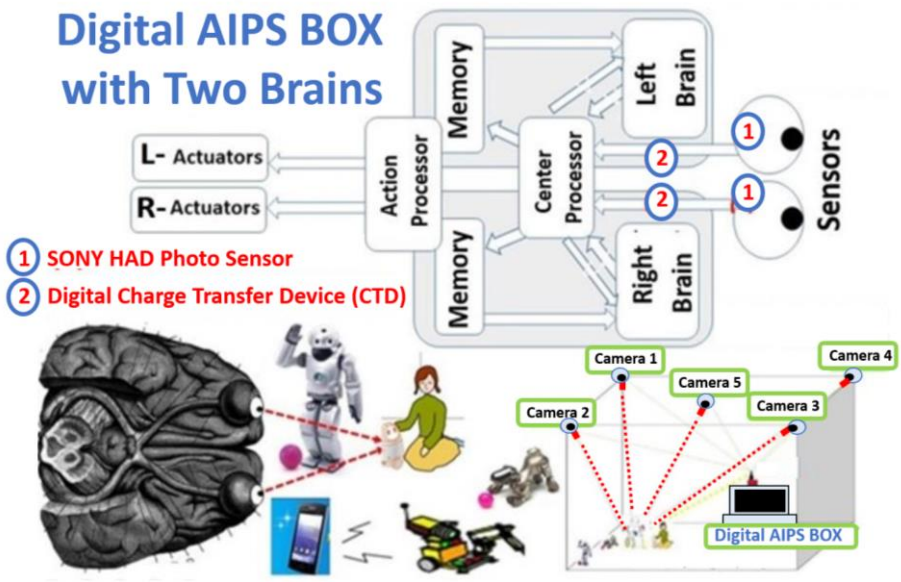

Figure 28. Artificial Intelligent Partner System (AIPS) introduced in 2008 by Sony.

FIFA's use of VAR at the 2022 World Cup in Qatar was different from the Premier League's use with the addition of a semi-automatic offside system as explained in details by the author in the SSIS ENCORE journal published in July 2023. The photo is an example of VAR photos.

The new element uses 12 dedicated cameras that tracks the ball and all players to calculate their exact position on the pitch. Each camera, installed under the roof of the stadium, receive 50 data points per second. They focus on 29 data points, including every limb of every player and the limbs needed for offside. The match ball will also provide a key element.

The pinned-surface buried-channel photodiode Sony invented in 1975 is now widely known simply as the pinned photodiode (PPD), which a shallow p-type or n-type (respectively) substrate layer, such that the intermediate buried diffusion layer can be fully depleted of majority carriers, such the base region of dynamic bipolar junction transistor [55–56].

The Sony original 1975 invention of the pinned-surface hole-accumulation diode (HAD), usually in the pinned-surface P+PNPP+ double junction type structure, is now used widely in CMOS active-pixel image sensors in world-wide in all digital and smartphone cameras; a precursor pinned-surface N+NPNPP+ triple junction variant with the MOS buffer capacitor for photo holes as the signal carriers and the back-light illumination scheme with complete charge transfer and no image lag was invented by Sony in 1975. This scheme was widely used in many image sensor applications now.

The artificial intelligent partner system (AIPS) of our future real-time high-performance computing system, inspired by Prof. C. A. Mead when I was a graduate student at Caltech in 1972 [57–59] is depending on the massive assemblies of parallel processors over mesh-connected wireless networks

to execute vast amounts of computational tasks with vast numbers of sensors of all types in order to assist the way humans and computers interact in order to meet our limit-less human needs. This real-time AI smart vision chip has a sun-light energy-sourced solar cell function capability utilizing a unique high-performance N × N pixel array of the pinned-surface P+PNPP+ double junction type Sony HAD sensors with the excellent photon-to-electron conversion efficiency and the highly light-sensitive image-sensor, now with a built-in solar cell capability, even at the very low light level, very much more super-sensitive than human eyes [60–62].

13. Summary and Conclusion

The buried-channel type charge coupled device (CCD) is not the only charge transfer device (CTD) that can transfer one single photo electron in the buried-channel N region, which is completely depleted of majority carrier electrons.

The pinned-surface buried-channel P+PNPP+ double junction photodiode can also transfer one single photo electron in the buried-channel N region, which is completely depleted of majority carrier electrons.

The charge transfer gate (CTG) and the pre-charge gate (PCG) are both chosen to be a depletion-type MOS transistor with a negative threshold gate voltage, so that in the external power-off mode, both of the N-type buried-channels under the CTG and the PCG MOS transistors are kept open for photo electrons to flow freely, for passing through to the outlet drain, which can be switched to the solar cell load.

Classical MOS type CTD image sensors suffered not only the serious image lag problem but also a large undesired CkT thermal noise and high frequency clock noise, degrading the picture quality. Due to these drawbacks, CCD type CTD type image sensors were widely used in image sensor applications, until late 1990s. Thanks to the advancement of CMOS scaled process technology, CCD is now completely replaced by the in-pixel source-follower current-amplifier type charge transfer device.

The double junction solar cell also has also a small-area outlet N+ drain region to connect the solar cell with the external load and the identical external maximum power tracking technology (MPTT) can be applied. Besides, the buried-channel N region, completely depleted of both majority carrier electrons and minority carrier holes, can transport even one single photo electron without recombination in the silicon chip for a long distance, directing photo electrons toward the small-area outlet N+ diffusion region, and very suited for high performance solar cell applications.

A new AI smart robot vision chip in the modern 3DIC CMOS image sensor technology is proposed, which is composed of an array of N × N pinned-surface buried-channel P+PNPP+ double junction type photo diodes, N × N analog-data steam mask-and-match comparators, and SRAM cache buffer CMOS memory units. All of them are integrated in a 3-D multichip system with the original 1972 basic architecture designed by Caltech EE graduate students.

In the external power-off mode, as an AI self-energy robot vision chip, the image sensor array of N × N pinned-surface buried-channel P+PNPP+ double junction type photo diodes can also function as a solar cell energy source unit. By a clever device and circuit design scheme, this array of N × N pinned-surface buried-channel P+PNPP+ double junction type photo diodes also function as a solar cell unit for the AI self-energy robot vision chip application. This real-time super performance solar cell in the AI smart robot vision chip is in this 3DIC multichip architecture with a unique high-performance unit of the built-in solar-cell and image-sensor combined SONY Hole Accumulation Diode (HAD) sensor type soalr device structure, which is based on the Sony original 1950s semiconductor process of

the P+PNPP+ double junction dynamic bipolar transistor technology with a charge transfer device unit which is based by the modern scaled CMOS 3DIC digital multichip process technology that Sony and many competing companies are developing.

The floating-surface single-junction N+NPP+ junction type photodiode with a typical depletion width $Wd = [X1, X2] = [0.2, 2.0]$ gives the efficiency of about 66.8 − 40.0 = 26.8%. However, in case of the P+P pinned-surface completely-depleted buried-channel Sony Hole-Accumulation Diode (HAD) sensor type solar cell, utilizing the high-energy ion implantation technology, if we achieve the depletion depth of $X2 = 3.0\ \mu m$, then, the solar cell efficiency of $80.4 - 34.7 = 45.7\%$ is expected. This expectation must be urgently examined and tested by fabricating a real silicon chip.

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James McCaldin at California Institute of Technology (Caltech) introduced and taught, in our undergraduate classes, the basic semiconductor device physics at Caltech in 1969 with plenty of side-wall back-ground exciting stories of Intel's unique self-aligned E/D MOS transistor technology and the newly developed high energy ion implantation technology.

C. A. Mead and T. C. McGill at Caltech advised the author the original 1971 undergraduate work on the Ga2O3-Au Schottky Barrier interface study and characterization, and also for guiding the Caltech 1974 PhD thesis work on the charge transfer analysis of buried channel CCD image sensors.

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Sony image sensor R/D efforts started in 1969 with the strong initiative of the ex-president of Sony Corporation, Kazuo Iwama, who emphasized the market need of the portable small video camera with the no image lag feature for the real-time fast-action-capturing and snap-shot pictures.

Kazuo Iwama gave the author a chance to work at Sony in 1975 to build an artificial intelligent image sensor system with real-time robot vision and the powerful digital circuit engines for real-time operations.

A long history of SONY bipolar process and device technology gave hints and guidance to the original 1975 inventions and also led to the 1978 successful development of the highly light-sensitive device.

Sony reported the complete charge transfer capability and the no-image-lag feature at the SSDM1978 conference in Tokyo. After a sequence of invited talks at the CCD1975 in Edinburgh Scotland UK in 1979 and at the IEEE ESC1980 conference in St. Louis USA, Sony kept silence and focusing on the efforts in the production and yield enhancement to improve cost-performance. With the understandings and encouragements by Sony president Norio Ohga and the top managements, Sony finally introduced the passport size portable video camera on the market in 1987 after 12 years of pains-taking hard diligent works by many people involved since the 1975 invention.

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snapshot full-size image capturing system for digital solid-state camera applications. The all-solid-state portable digital camera, which was completely free of any film-media and mechanical parts, opened the gate way to the modern high-definition digital TV and the smart-photon electronic imaging eras.

Conflicts of interests

The author declares no conflict of interest.

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