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An 8-channel high-voltage neural stimulation IC design with exponential waveform output

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Abstract: This paper presents the design of a high-voltage 8-channel neural stimulation integrated circuit with exponential-waveform output. To ensure sufficient current delivery to the load, which exhibits large impedance at the electrode-tissue interface, a high-voltage output stage of up to 30 V has been implemented in the neural stimulator. Charge balancing is achieved through a dual-slope control scheme with an integrator circuit during stimulation, complemented by an additional active charge-balancing circuit in each channel. This work also demonstrates that the stimulator with exponential-waveform output remains effective even with a high-voltage output stage and is compatible with traditional charge-balancing circuits. These features ensure safety and higher power efficiency in long-term stimulation. The 8-channel high-voltage stimulator chip is implemented using 180-nm BCD CMOS process technology, with a core area of 13.25 mm ². Experimental measurements indicate that the maximum charge imbalance for a single cycle is only 0.77%, while the output power efficiency can reach 98%. *In vitro* and *in vivo* experimental results show that the stimulator effectively removes residual charges, and the exponential-waveform stimulation successfully triggers action potentials leading to muscle contraction.

Keywords: Neural stimulation; high-voltage; multi-channel; exponentially decaying current; charge balancing

1. Introduction

Neural modulation technology can treat illnesses such as Parkinson's disease, epilepsy, and motor function loss caused by spinal injuries [1–3]. The essence of closed-loop neural modulation or brain-machine interface (BMI) is to analyze and evoke electrical signals within the nervous system [4]. The neurostimulation chip is an indispensable module in neural modulation and BMI, responsible for delivering and discharging electrical charges to neurons and facilitating the transmission of electrical signals within cells. For example, as shown in Figure 1, during the stimulation process, electrons enter the extracellular fluid through the stimulation electrode, lowering the extracellular potential. When the transmembrane potential reaches the threshold, an action potential (AP) is generated, and ion channels on the cell membrane open. K^+ or Ca^{2+} ions exit the cell until the transmembrane potential returns to its resting state. This highlights the importance of charge balancing in neural stimulation, as residual charge in the extracellular space can lead to ion imbalance and tissue damage. Therefore, the neural stimulation integrated circuit (IC) must incorporate charge-balancing mechanisms to ensure safety [5–8].

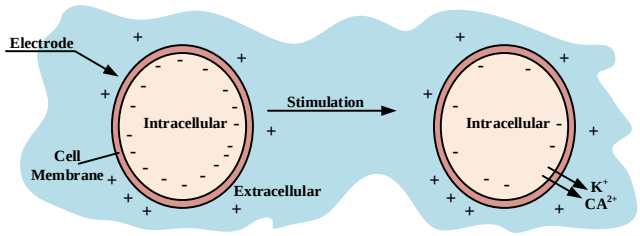

Figure 1. Principles of neural stimulation in a cell-level view.

Unlike single-channel neural stimulators, biomedical devices with multi-channel neural stimulation chips offer advantages in terms of functionality, size, and cost-effectiveness in the treatment of neural regulation and the repair of auditory, visual, motor, and other nerves. Therefore, the design of multi-channel stimulators has become a key focus of research [9–13].

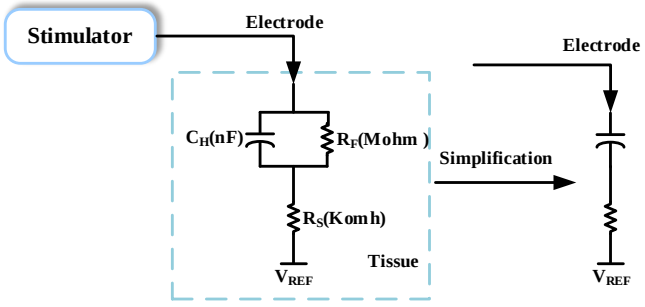

Figure 2. Electrical model of electrode-tissue interface.

The equivalent model for the electrode-tissue interface in neural stimulation is shown in Figure 2. It consists of a Helmholtz capacitance (CH), Faraday resistance (RF), and an electrolyte solution resistance (RS) [14]. RS is determined by the concentration of cell fluid in different nerve tissues, typically in the kilo-ohm range. RF is the additional impedance

caused by electrochemical and concentration polarization during ion exchange. Due to the large magnitude of RF, it is generally considered equivalent to an open circuit. Therefore, the electrode model is usually simplified to a series-connected capacitor (CH) and resistor (RS). This configuration determines the voltage waveform at the load when stimulation current flows through the electrode-tissue interface.

With the emergence of increasingly miniaturized implantable chips, the production and use of microelectrodes and flexible electrodes are also increasing, resulting in a significant increase in the characteristic impedance of the electrode-tissue interface. To ensure that sufficient charge can be delivered to the tissue through these high-impedance electrodes, it becomes necessary to increase the supply voltage of the output stage of the neural stimulation chip into the high-voltage range [5,13,14,15].

To prevent the accumulation of charges and tissue damage during neural stimulation, biphasic current or voltage stimulation waveforms are preferred [5–17]. To further enhance efficiency, stimulators with exponential-waveform output have also been proposed [18–20]. A comparison of output waveforms for constant-current and exponential-current stimulation is shown in Figure 3 [21]. Compared with constant-current stimulation, exponential-current stimulation offers higher power efficiency [20]. Considering the recent advances in current stimulation, from a biostimulation perspective, constant-current and exponential-current stimulation are better aligned with the development of high-voltage and high-density stimulators [5,11,13,20]. Moreover, due to the growing demands of implantable devices, the need for low power consumption is increasing significantly, and a conflict arises between achieving high density and maintaining low power consumption. Therefore, a single channel must achieve higher power efficiency to satisfy the overall low-power consumption requirements.

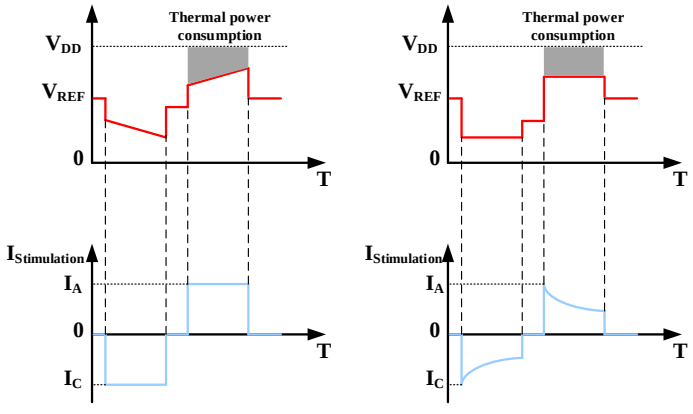

Figure 3. Comparison between constant-current stimulation and exponential-waveform stimulation.

In terms of current matching, researchers quickly discovered the shortcomings of conventional bipolar stimulation chips. Although using bipolar current can eliminate accumulated charges, the semiconductor process itself introduces a deviation of 0.1% to 1%, which does not ensure that the currents produced by the positive and negative current sources

are equal. As a result, this leads to the gradual accumulation of residual charges at the electrode-tissue interface. Such accumulation occurs in both biphasic rectangular and exponential waveform stimulators. In particular, exponential waveform stimulators face challenges due to the varying impedances at the electrode-tissue interface during cathodic and anodic stimulation phases, which may result in variations in impedance and the time constant of the load, rendering charge balancing difficult to achieve [5,11,13]. Due to the existence of non-ideal factors such as the fabrication process and stimulation mode, charges may remain after the stimulation of the electrode model, potentially leading to adverse effects. Therefore, charge balance is required to ensure the safety of stimulation.

Taking into account all design factors previously discussed, such as charge balancing, the number of stimulation channels, load model, supply voltage of the output stage, and current matching, we propose a neural stimulation chip design that addresses these requirements. A charge-balanced 8-channel high-voltage neural stimulator with exponential-waveform output is implemented. In this design, accounting for the impedance changes during cathodic and anodic stimulation, the RC time constant of the exponential current is designed to be independently adjustable to achieve high power efficiency in both phases. To ensure sufficient charge transfer, this IC uses a high-voltage output stage that can operate normally under a supply voltage of up to 30 V. Additionally, to guarantee safety, this study employs a dual-slope control scheme for synchronous charge detection to achieve delivered charge matching, combined with an active charge balancing circuit to minimize the residual charge. The rest of the paper is organized as follows: Section 2 describes the proposed neural stimulator system architecture. Section 3 provides the design details of each circuit in the neural stimulation IC. Section 4, Section 5 and Section 6 present the measurement results from benchtop, *in vitro* (phosphate-buffered solution, PBS), and animal experiments, respectively. Section 7 presents the conclusion of this study.

2. System architecture

Figure 4 shows the system architecture of the proposed 8-channel high-voltage neural stimulation IC. Each channel of the neural stimulator contains a current waveform generation circuit, a high-voltage output driver, a parallel proportional current reducing circuit, and a synchronous charge integration circuit for charge balancing control, a voltage detection circuit, and a short-time pulse insertion circuit for active charge balancing. The bandgap circuit and logic control circuit are shared by all channels. The entire system is powered by multiple supply voltages of 1.8 V, 3.3 V, and a high voltage (up to 30 V, external).

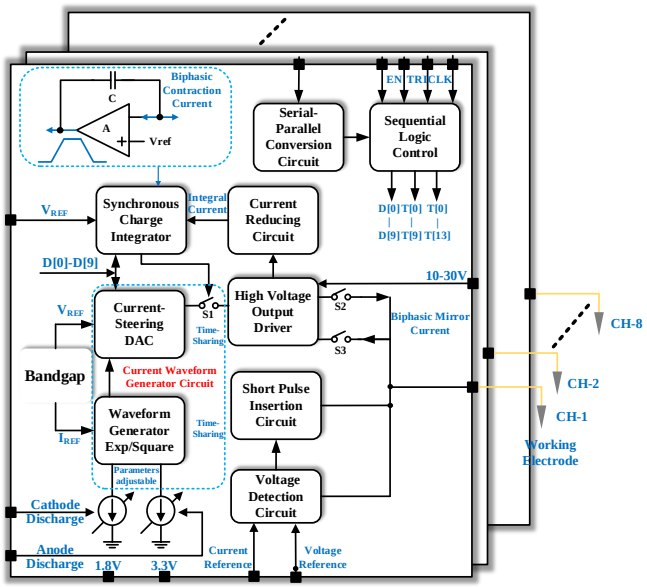

Figure 4. The system architecture of the proposed 8-channel high-voltage neural stimulation IC with improved safety.

The current waveform generation circuit consists of a 10-bit current steering DAC and an exponential or square waveform generation circuit, which can operate in either constant-current output mode or exponential-current output mode. During different stimulation phases, cathodic and anodic discharge current sources (connected to the waveform generator in Figure 4) can be adjusted to produce exponential currents with varying time constants. The reference current generated by the waveform generation circuit converts the single-phase current into a bidirectional current through a high-voltage driver, thereby enhancing the current driving capability, allowing for an output voltage of up to 30 V. The synchronous charge integration circuit and the proportional current reduction circuit form a synchronous charge detection system, which is responsible for managing the charge balance process within 700 µs of the pulse. If the pulse width is set to 700 µs or larger (up to 10 ms), then charge balancing is managed by the digital counters in the logic control circuit, and the synchronous charge integrator module is disabled. The short-time pulse insertion circuit ensures that the charges in the neural tissue are within a safe range, while the sequential logic control circuit schedules and allocates the circuit structure. The eight channels are independent of each other, allowing control over activation and deactivation while adjusting the corresponding stimulation parameters to adapt to the characteristic impedance of the electrode-tissue interface at various stimulation sites. The neural stimulation parameters can be set externally and sent to the chip's serial-to-parallel conversion circuit. Then, the sequential logic control circuit sets the internal stimulation parameters of the chip. The detailed circuit implementation is illustrated in Section 3.

3. Circuit implementation of the neural stimulator

3.1. Current waveform generation circuit

In exponential-waveform current stimulation, to ensure that the stimulator maintains a constant voltage at the load during the stimulation phase while achieving higher power efficiency, the exponential current should meet the following requirements [20]:

$$I_{(t)} = I_0 e^{\left(-\frac{t}{R_S C_H}\right)} \tag{1}$$

Based on the result of formula (1), the time constant (τ=RSCH) must match the characteristic impedance of the electrode-tissue interface [20]. The current waveform generation circuit proposed in this paper is divided into two components: the waveform generation circuit and the current steering DAC. The waveform generation circuit is responsible for generating exponential waveforms, while the current steering DAC produces the initial amplitude of the stimulation current. The current waveform generation circuit can offer two output modes: exponential-current stimulation and constant-current stimulation.

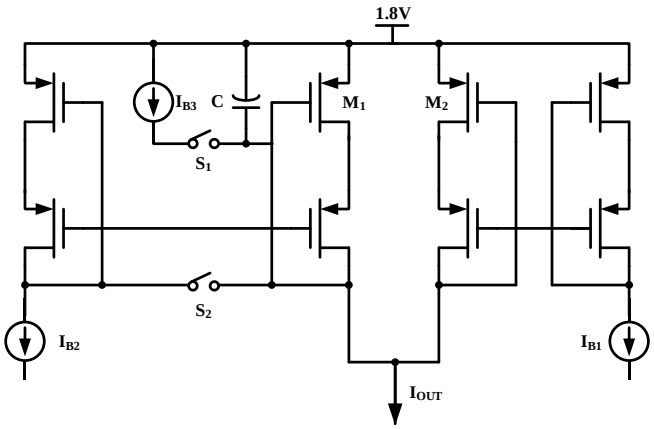

Figure 5. Waveform generation circuit.

The waveform generation circuit proposed in this paper is illustrated in Figure 5 and consists of two constant current sources (I_{B1} and I_{B2}), an adjustable current source (I_{B3}), a capacitor (C) for voltage storage, a CMOS switch (S_1), a waveform selection switch (S_2), and a series of wide-swing cascode current mirrors. I_{B1} and I_{B2} are unequal constant current sources, with $I_{B1} > I_{B2}$, serving as gate voltage supplies for M_1 and M_2. Capacitor C is used as an energy storage element, and I_{B3} is a discharge reference current source that adjusts the output amplitude. It can change the discharge time constant of the exponential decay current to match different electrode impedance models. The exponential current is generated by summing the constant current from the PMOS transistor in the saturation region with the time-variant current from transistor M_1. The approximate equation for the exponential current derived from a Taylor series quadratic expansion is as follows:

$$I_{(t)} \approx I_0 \left[1 - \frac{t}{R_S C_H} + \frac{1}{2!}\left(\frac{t}{R_S C_H}\right)^2\right] \tag{2}$$

Subsequently, further simplification can be expressed as follows:

$$I_{(t)} \approx \frac{I_0}{2}\left[1+\left(1-\frac{t}{R_S C_H}\right)^2\right] \tag{3}$$

Let the difference between V_{gs1} and V_{gs2} as A. The output current of the circuit illustrated in Figure 5 can be expressed as follows:

$$\begin{aligned} I_{OUT} &= \frac{\beta}{2}\left(V_{gs2}+A-V_{th}-\frac{I_{B3}t}{C}\right)^2+\frac{\beta}{2}\left(V_{gs2}-V_{th}\right)^2 \\ &= \frac{\beta}{2}\left(V_{gs2}-V_{th}-\frac{\mathrm{AC}+I_{B3}t}{C}\right)^2+\frac{\beta}{2}\left(V_{gs2}-V_{th}\right)^2 \\ &= \frac{\beta}{2}\left(V_{gs2}-V_{th}\right)^2\left[1+\left(1-\frac{I_{B3}\left(t-\frac{AC}{I_{B3}}\right)}{C\left(V_{gs2}-V_{th}\right)}\right)^2\right] \end{aligned} \tag{4}$$

By comparing (3) and (4), we can conclude that exponential current generation occurs when the two expressions are identical. Thus, it can be further simplified as follows:

$$\begin{aligned} I_{OUT} &= \frac{\beta}{2}\left(V_{gs2}-V_{th}\right)^2 e^{-\frac{I_{B3}\left(t-\frac{AC}{I_{B3}}\right)}{C\left(V_{gs2}-V_{th}\right)}} \\ &= \frac{\beta}{2}\left(V_{gs2}-V_{th}\right)^2 e^{\frac{A}{C\left(V_{gs2}-V_{th}\right)}} e^{-\frac{I_{B3}t}{C\left(V_{gs2}-V_{th}\right)}} \end{aligned} \tag{5}$$

When the initial gate voltages of M_1 and M_2 are equal, equation (5) can be further simplified to:

$$I_{OUT} = \frac{\beta}{2}\left(V_{gs2}-V_{th}\right)^2 e^{-\frac{I_{B3}t}{C\left(V_{gs2}-V_{th}\right)}} \tag{6}$$

Given the application of Taylor expansion to progressively approximate the exponential current, it is essential to assess the accuracy of the exponential decay current. In this study, we permit a relative error margin of 5% between the ideal exponential curve e^x and the quadratic approximation curve, resulting in the following range for the calculated x:

$$-0.8 < x < 0.57 \tag{7}$$

The variable x also represents the time constant of the exponential current. Given the constraint condition $-0.8 \leq x$, we can correlate it with the circuit parameters:

$$-0.8\frac{\left(V_{gs2}-V_{th}\right)}{I_{B3}} \leq -\frac{A\times C}{I_{B3}}\left(x=0\right) \tag{8}$$

Further simplification yields the following:

$$A \leq 0.8\left(V_{gs2}-V_{th}\right) \tag{9}$$

Previously, we defined V_{gs1}-V_{gs2}=A; by substituting and simplifying, we can derive the following:

$$\left(V_{gs1}-V_{th}\right) \leq 1.8\left(V_{gs2}-V_{th}\right) \tag{10}$$

For the MOS drain current, as described by the square law formula:

$$I_{B1} = \frac{\beta}{2}\left(V_{gs1} - V_{th}\right)^2 \tag{11}$$

$$I_{B2} = \frac{\beta}{2}\left(V_{gs2} - V_{th}\right)^2 \tag{12}$$

This leads to a quantitative relationship between I_{B1} and I_{B2}:

$$I_{B1} \leq 3.24 I_{B2} \tag{13}$$

In this design, we set $I_{B1} = 3I_{B2}$. The current generated by the waveform generation circuit is subsequently supplied to the current DAC, allowing for different current stimuli to be achieved through various DAC configurations.

In the context of the exponentially decaying current waveform, another critical factor is that the time constant of this exponential current must align with the characteristic impedance of the electrode-tissue interface. The characteristic impedance of the electrode-tissue interface varies based on the stimulation site and the electrode material employed. Consequently, it is essential to adjust the current value of I_{B3} to achieve time constant matching with varying characteristic impedances. According to Formula (6), the condition required for achieving time constant (τ) matching is:

$$\tau = \frac{C\left(V_{gs2} - V_{th}\right)}{I_{B3}} = R_S C_H \tag{14}$$

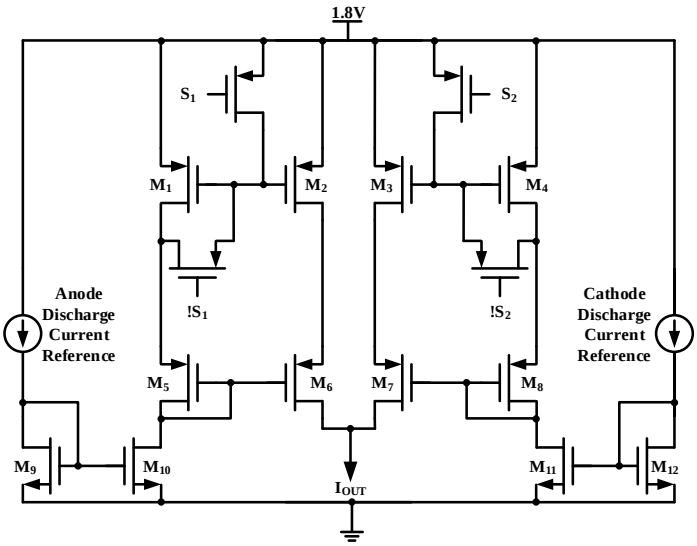

Figure 6. Impedance matching circuit.

For a specified capacitor C and a constant current source I_{B2}, impedance matching can be achieved by adjusting the value of I_{B3}. The output current of the current waveform generator can be adjusted by modifying the value of the current source illustrated in Figure 4, thereby achieving impedance matching for both the cathode and anode. However, variations in electrode impedance resulting from electrochemical reactions within the tissue typically lead to differing impedances during the cathodic and anodic stimulation phases, necessitating distinct charging currents $I_{B3}$for each phase. The adjustment of I_{B3} is typically performed

during the interphasic delay phase. The impedance matching circuit is illustrated in Figure 6; this circuit allows for the charging current I_{B3} during the cathodic stimulation phase to operate independently from that in the anodic stimulation phase. The anode and cathode discharge references are provided off-chip and are both adjustable. Digital signals S_1 and S_2 are supplied by the sequential logic control circuit, and the reference current is switched during the interphase delay phase to ensure the discharge currents I_{B3} during both cathodic and anodic stimulation phases are independent of each other. Due to the substantial impedance of the electrode-tissue interface, a small discharge current I_{B3} is required, typically at the nanoampere (nA) level. The resistance RS typically ranges from tens to hundreds of kilohms; (V_{gs2}-V_{th}) is in the millivolt (mV) range, C_H is at the nanofarad (nF) level, and ccc is at the picofarad (pF) level. Consequently, a current reduction circuit is required to attenuate the reference current before supplying it to the waveform generation circuit. The schematic of this circuit is illustrated in Figure 7. This reduction circuit operates on the principle of shunting, leveraging the resistance characteristics of transistors. By manipulating the dimensions of the transistors, a current reduction ratio ranging from hundreds to thousands can be achieved.

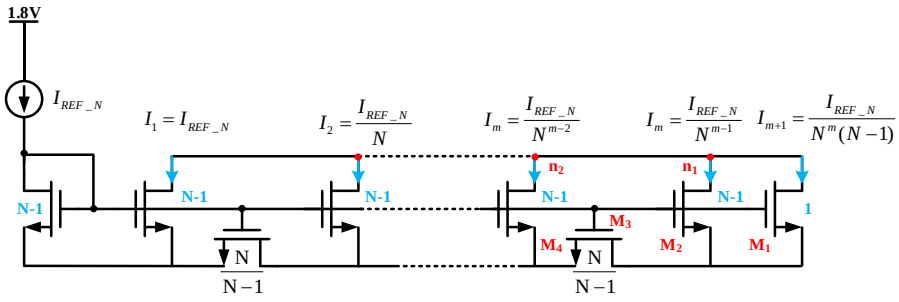

Figure 7. Current reduction circuit.

In this design, the current-mode neural stimulators necessitate a DAC to regulate the stimulation current, ensuring that the output current achieves a broad range suitable for varying impedances. The DAC is divided into two internal groups, employing a mixed decoding method. The lower three digits are binary-encoded (1 LSB), while the upper seven are decoded using a thermometer code (MSB = 8 LSB). The circuit employs a row and column decoding structure comprising 16 rows and 8 columns, which includes a 3–7 decoding circuit, a 4–15 decoding circuit, and 127 basic current units. Consequently, the final output current of the stimulator ranges from 1 μA to 1 mA.

In the context of stimulation strength settings for multi-channel applications, a series-to-parallel conversion circuit is required to reduce the number of electrode pads utilized. This configuration enables the external transmission of serial data to each individual channel of the stimulator, thereby optimizing the stimulation setup.

3.2. High-voltage output drive circuit

The emergence of various types of microelectrodes and flexible electrodes has led to an exponential increase in the characteristic impedance of the electrode-tissue interface. Therefore, it is essential to increase the supply voltage of the output stage of the stimulator chip to a high-voltage domain to ensure sufficient charge delivery, without reducing the amplitude of the stimulation current. As illustrated in Figure 8, when the supply voltage of the output stage is increased to the high-voltage domain (i.e., 10–30V), all transistors, except for the control switches, are constructed using the 30-V BCD process to ensure optimal performance of the output stage in this domain. The electrodes utilized in subsequent tests were composed of a platinum-iridium alloy, exhibiting a CH value at approximately the nF level and an RS value at approximately the kΩ level. The input current of the high-voltage output driver corresponds to the output current of the front-stage DAC. Subsequently, this current from the DAC is converted into source and sink currents through high-voltage current mirrors, which direct the currents to the electrode via the output port. The direction of the output current can be controlled using the control signals S_A and S_C to achieve the biphasic current stimulation function. Furthermore, the output currents are scaled down to I_A and I_C, which flow into the synchronous charge detection circuit for dual-slope charge balancing control [23].

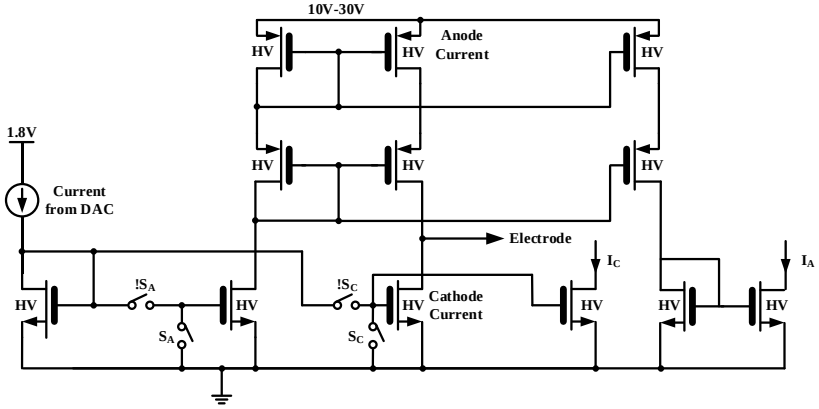

Figure 8. Circuit of high-voltage output driver.

3.3. Bandgap reference circuit

The primary function of the bandgap reference circuit is to supply bias current, reference current, and reference voltage within the chip. As illustrated in Figure 9, this module primarily comprises a PTAT currdacent generation circuit, a bandgap reference voltage generation circuit, and a voltage-to-current conversion circuit. The primary function of the PTAT current generation circuit is to provide bias current for the operational amplifier and comparator within the chip. As the temperature increases, carrier mobility decreases, and the PTAT current exhibits a positive temperature coefficient to offset this effect, thereby ensuring that the gain and bandwidth of the operational amplifier remain relatively stable across temperature variations. The function of the bandgap reference voltage generation circuit is to produce temperature-independent voltages, which serve as the bias voltage for

the wide-swing cascode current mirror and the reference voltage for the voltage-to-current conversion circuit. The current-steering DAC requires its reference current to be temperature-independent; thus, the function of the voltage-to-current conversion circuit is to convert the temperature-independent voltage into a temperature-independent current. To mitigate significant resistance variations across different process corners, two resistors are connected in series, and two digital signals are employed to fine-tune the resistance value and adjust the reference current. This module follows the classic current-mode bandgap reference design; hence, further elaboration is unnecessary.

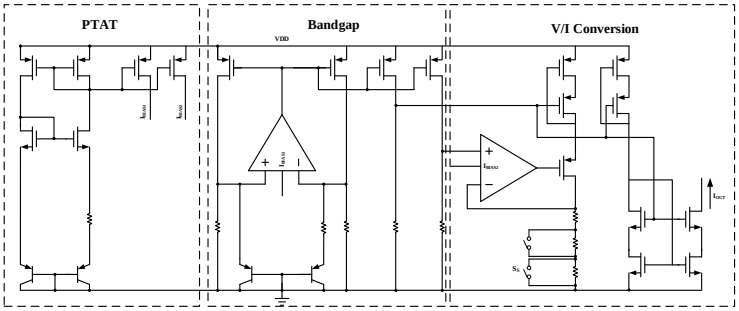

Figure 9. Circuit of Bandgap reference.

3.4. Charge balance circuit

Constant-current neurostimulators utilize biphasic currents to stimulate the electrode-tissue interface, and when the timing and amplitude of both cathodic and anodic stimulation currents are identical, theoretically, no residual charge remains, which is the traditional charge balance method of current stimulators. However, in modern current stimulation modes, practical considerations result in varying amplitudes between the cathodic and anodic currents. Thus, complete charge equilibrium cannot be achieved solely by using a clock to control the stimulation time. By controlling the amount of residual charge in a single cycle and promptly removing it, charge balance can be maximized. In this article, a synchronous charge detection circuit and a short-pulse insertion circuit are employed to jointly achieve charge balance. The synchronous charge detection circuit controls the amount of residual charge in a single stimulus, while the short-pulse insertion circuit removes the residual charge in a timely manner. Together, these circuits ensure that the stimulator's residual charge remains within safe limits during long-term and multi-cycle operations.

Figure 10 presents the system diagram of the synchronous charge monitoring circuit. In the synchronous charge detection circuits, the reference current is derived from the proportional current of the stimulation current, as discussed earlier regarding the current reduction circuit. Once the reference current enters the system, it is fed into a synchronous integration circuit comprising a switched-capacitor integrator and a comparator. The output of the synchronous integration circuit is regulated by a feedback loop to govern the operational state of the stimulator. Figure 11 illustrates the timing of the stimulator's operation within the charge balance circuit. Initially, when SC is closed, the system enters the cathodic current stimulation phase. Due to the sink current of the cathode, charge flows out of

the synchronous integration circuit. When SC is disconnected, the system enters the phase delay stage, during which the stimulator ceases to output current, allowing time for the action potential (AP) generated by the cathodic stimulation current to propagate to the neural unit. Subsequently, when SA closes, the system enters the anode current stimulation phase. The source current generated in this phase injects charge into the synchronous integrator circuit. The charge balance process is observed in the integration circuit. Once the remaining charge reaches zero, the voltage comparator's potential flips, and this signal is fed back to the digital logic circuit, turning off SA and concluding the charge balance. Subsequently, to promptly remove residual charge during the active charge balancing phase, active charge balancing-compared to traditional passive methods-offers advantages in both speed and accuracy. Switch S0 serves as the reset switch of the synchronous charge detection circuit. When S0 is closed, it connects the integrator to a unity-gain amplifier, restoring the output voltage to the reference point. Notably, in this work, both the cathodic stimulation time and phase delay time are clock-controlled, whereas the anodic stimulation time can be governed by either the synchronous charge detection circuit or the clock. The submodules of this circuit were introduced in the previous section; therefore, this part focuses solely on the synchronous charge detection process. Figure 11 should be viewed in conjunction with Figures 10 and 12, which depict the operating timing of the switch in Figure 10 and the voltage status of each node.

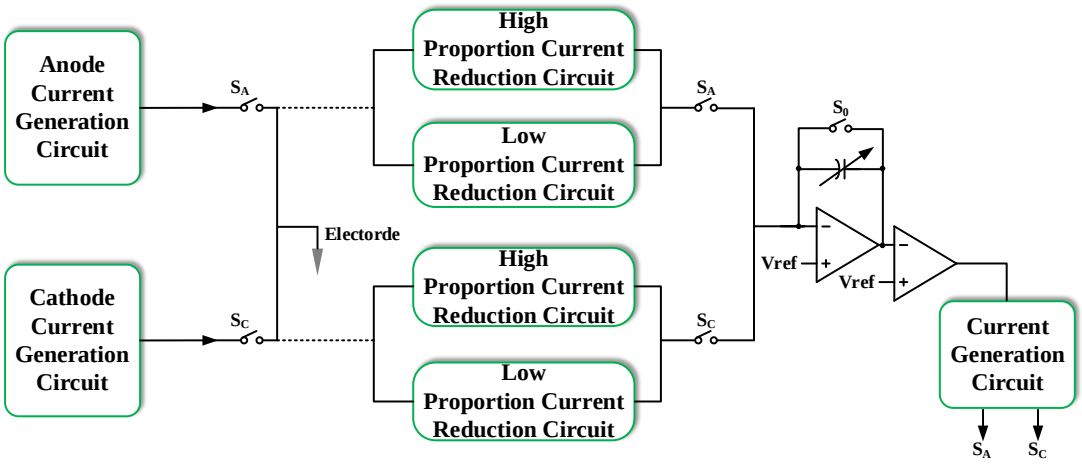

Figure 10. Synchronous charge monitoring circuit.

In this study, the accuracy of the synchronous charge detection circuit is ensured through two primary methods. First, the reference current for the synchronous charge detection circuit is derived from the scaled-down stimulation current, which significantly differs from the stimulation current (in the nF range). When using the proportional reduction and synchronous integration circuits, the integration current may become too low, significantly affecting the detection accuracy of the synchronous charge detection system. Therefore, the stimulation current is divided into two groups based on its amplitude. A low-scaling current reduction circuit is used for low current inputs, while a high-scaling current reduction circuit is employed for high current inputs to preserve the accuracy of the synchronous charge

detection system. Second, the integrating capacitor in the integration circuit consists of an array of capacitors with varying capacitance values, allowing the capacitor size to be adjusted based on the stimulation current amplitude. This ensures that, even under different integration currents, the integration voltage remains approximately constant.

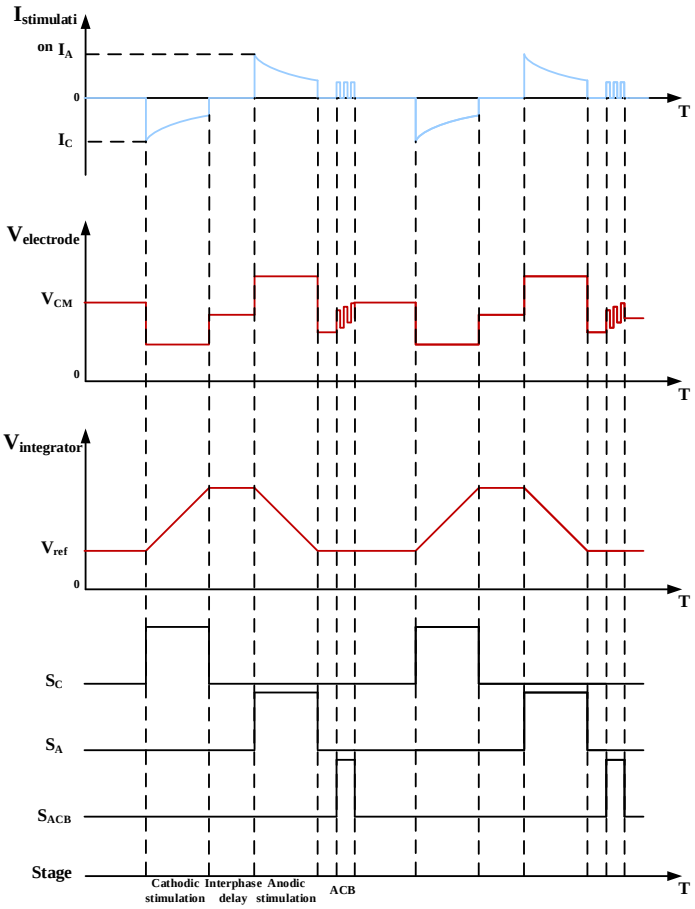

Figure 11. The timing of the stimulator operation.

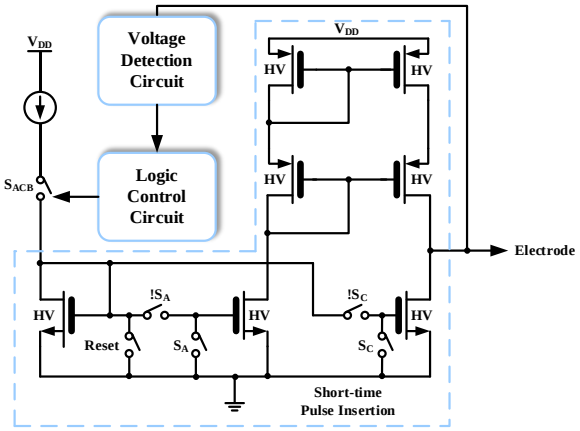

Figure 12. Circuit of active charge balancing module.

When the neural stimulator operates continuously, residual charge accumulation must be effectively managed. To remove residual charges reaching a threshold and avoid charge accumulation over multiple cycles, this study implements an active charge balancing system.

The active charge balancing system is illustrated in Figure 12 and consists of a voltage detection circuit, a logic control circuit, and a short-time pulse insertion circuit. First, the change in electrode voltage is measured via capacitive voltage division. The voltage signal is then transferred from the high-voltage domain to the low-voltage domain, where a comparator determines if the electrode voltage has returned to the reference potential after single-cycle stimulation. If the electrode voltage does not return to the reference potential, the system determines whether positive or negative compensation is needed, and a control signal is generated. Based on the monitoring circuit's output, short pulses are inserted into the circuit, delivering a series of brief current pulses to the electrode. Each pulse transfers a small charge to the electrode-tissue interface, gradually driving the neural tissue towards charge equilibrium. The frequency of these pulses, determined by the delay circuit within the monitoring system, is approximately hundreds of nanoseconds. The logic control circuit manages the initiation and termination of short pulse insertion. The active charge balancing system ensures the long-term operation of the neurostimulation chip, enhancing the safety and reliability of the implantable device.

4. Bench-top measurement results

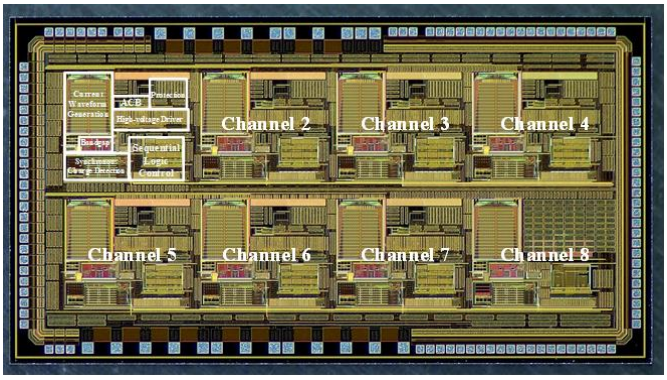

Figure 13. Die photo of the implemented neural stimulator chip.

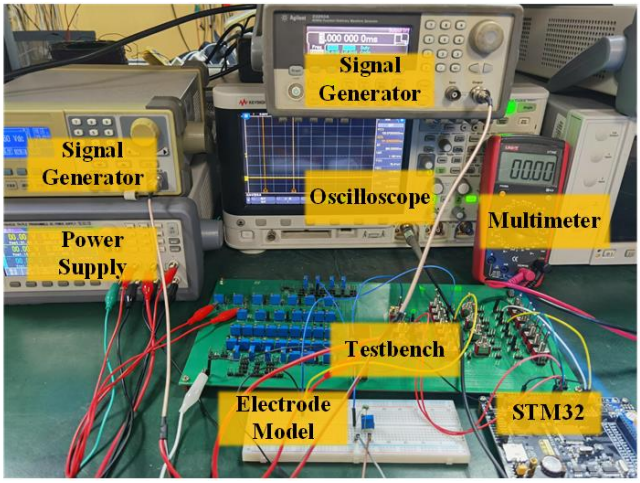

Figure 14. Bench-top testing environment.

The 8-channel high-voltage neural stimulator is fabricated using SMIC's 18-nm BCD CMOS process. Figure 13 presents the die photograph of the proposed neural stimulator. The chip occupies an area of 13.25 mm^2 (2.65 mm × 5 mm), with a core module area of 8.17 mm^2 (1.9 mm × 4.3 mm) and a single-channel area of approximately 0.96 mm^2 (1.039 mm × 0.921 mm).

The 8-channel neural stimulation chip was tested in a laboratory environment, as depicted in Figure 14. The instruments used in the test included a power supply, oscilloscope, multimeter, signal generator, STM32 development board, and a PCB test board with several discrete components. After adjusting the external biases of the PCB test board, the neural stimulation chip was powered, and its current output was measured. The test results are presented in Figure 15.

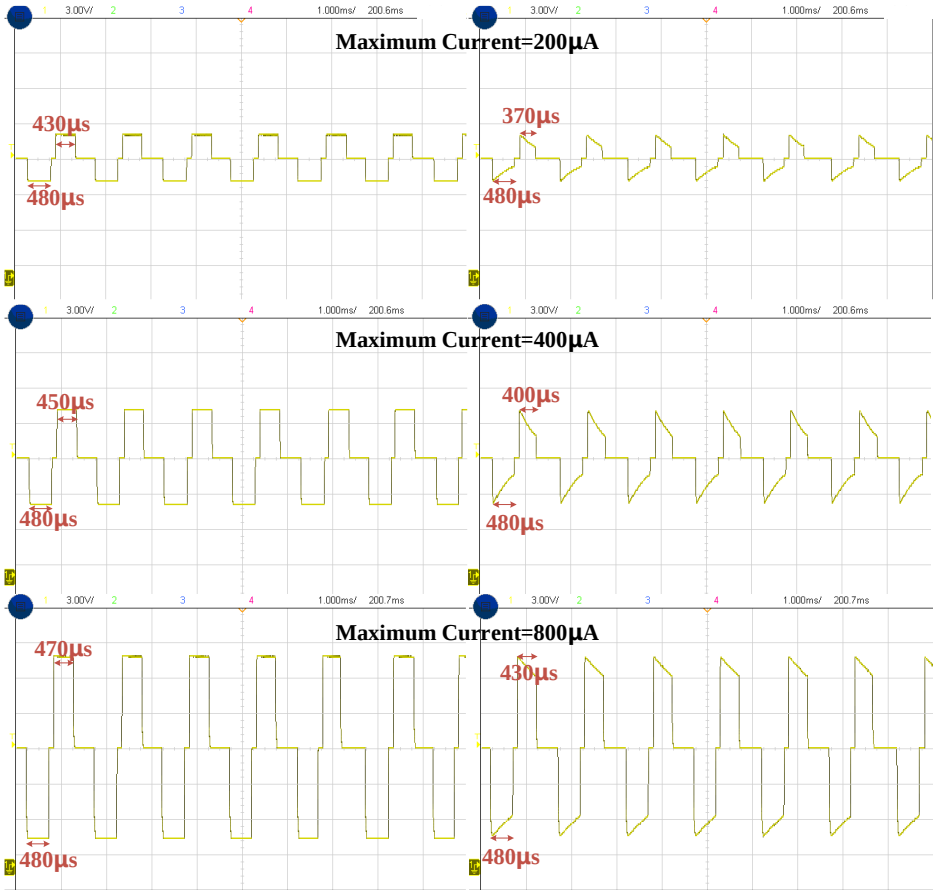

Figure 15. Resistance test results.

The load of the neural stimulation chip is a pure resistance of 10 kΩ, and the anode stimulation time is controlled by a synchronous charge detection circuit. By adjusting the input signal of the DAC, biphasic exponential and constant current waveforms with varying amplitudes can be obtained. The cathode and anode stimulation states are stable, the chip functions normally, and it can continuously trigger multi-cycle stimulation current outputs. Since Figure 15 is based on tests in a purely resistive load environment, residual charge accumulation will not be observed. However, the functionality of the synchronous charge detection circuit can be inferred by comparing the anode and cathode stimulation times.

When the cathode current differs from the anode current (due to variations in DAC settings and process mismatches), the difference in cathode and anode stimulation times indicates that the synchronous charge detection circuit can still achieve charge balance despite the mismatch between the two-phase currents.

The load of the nerve stimulation chip was replaced with a different electrode model, and the measurement results are presented in Figure 16. The stimulator operates in an exponential current output mode, with three sets of waveforms obtained from different test channels. The solution resistances RS are 10 kΩ, 20 kΩ, and 40 kΩ, corresponding to maximum stimulation currents of 750 μA, 420 μA, and 200 μA, respectively. The waveforms indicate that the stimulator achieves impedance matching with different electrode models, and the short-time pulse insertion circuit operates normally, effectively removing the residual charge promptly. The system maintains a constant electrode voltage during multi-cycle stimulation, achieving a stable safety state without any observable accumulation of residual charge.

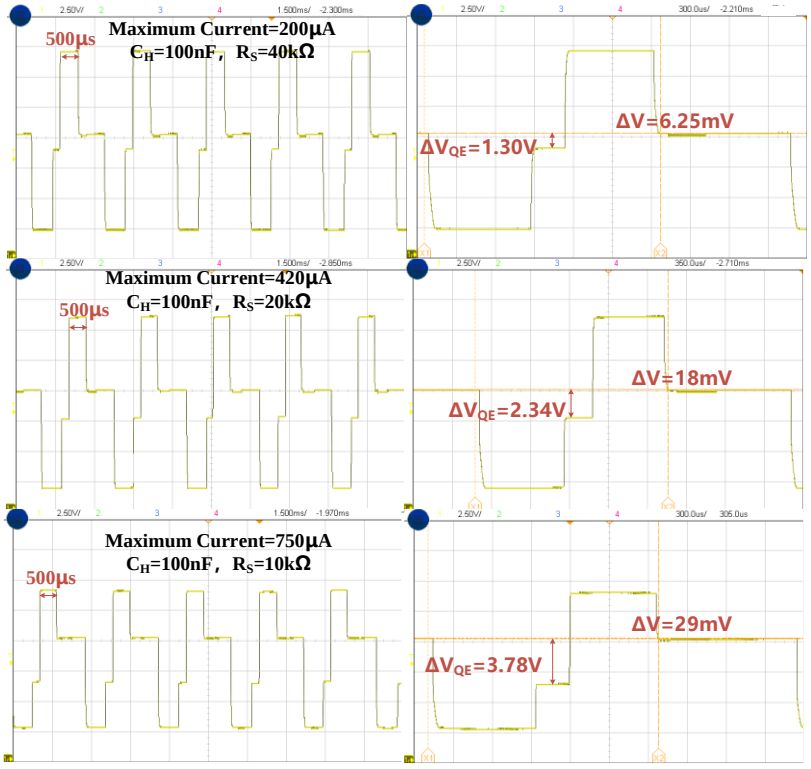

Figure 16. Test results based on electrode model.

The residual charge value can be calculated by measuring the difference in electrode voltage before and after stimulation, along with the Helmholtz capacitance (CH>) of the electrode model. The calculation formula is as follows:

$$Q_{residual} = C_H \times \Delta Velectrode \quad (15)$$

According to Equation (15), the remaining charges at three different electrode impedances are 2.9 nC, 1.8 nC, and 625 pC. Similarly, the mismatch between the remaining charge and the injected charge can be calculated using the peak electrode voltages, which are 0.76%, 0.77%, and 0.48%, respectively. Figure 17 illustrates the charge mismatch of the same electrode model under different initial stimulation currents. The test results

demonstrate that this work has achieved significant charge balance performance. Given the variations in stimulation current, the absolute value of the residual voltage is less significant; thus, the ratio of residual charge to injected charge is of greater importance.

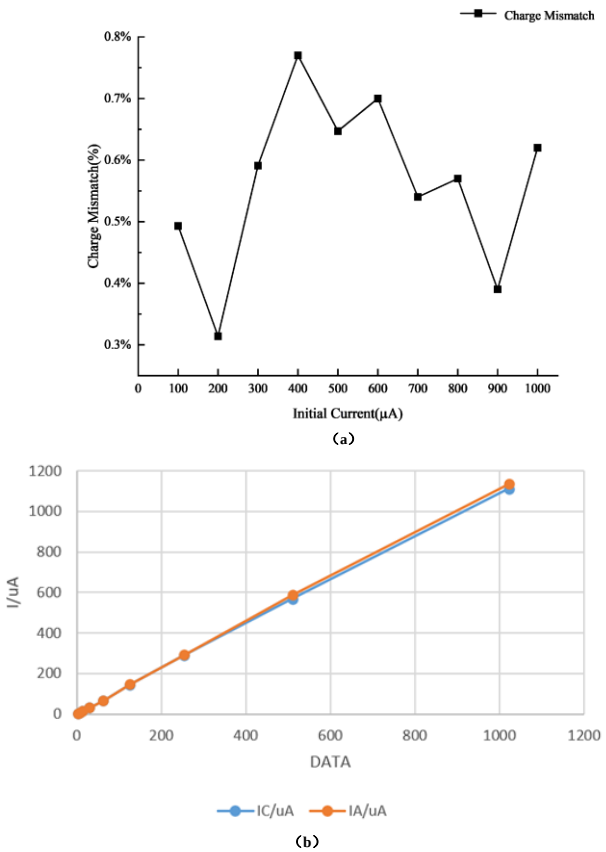

Figure 17. (a) Test result of charge mismatch v.s. stimulation current amplitude; (b) Test results of output current for DAC and High-Voltage Output Drive Circuit.

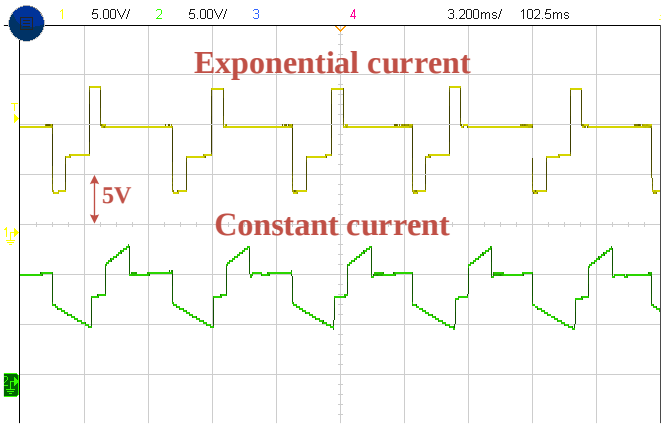

Figure 18. Waveforms of 2-channel parallel stimulation.

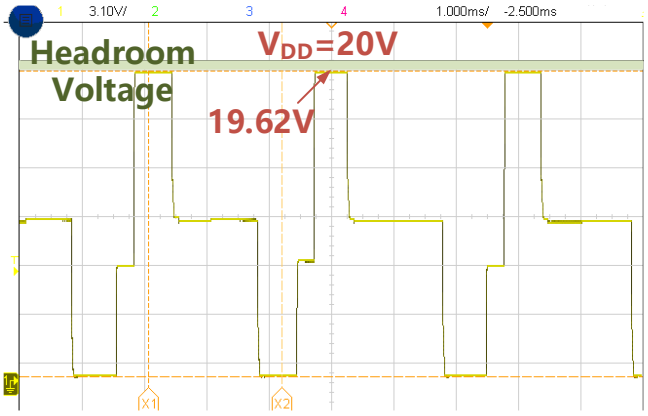

Figure 19. Voltage waveform at the output (to test Maximum power efficiency).

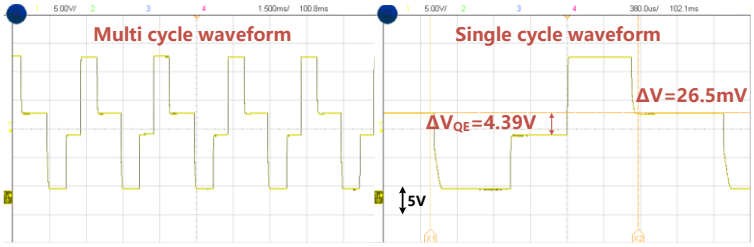

Figure 20. Exponential stimulus waveform at a working voltage of 30 V.

Figure 18 illustrates the motor voltage waveform when two channels are operating simultaneously. The data indicate that the isolation between channels is effective, verifying the stability of independent operation among multiple channels. The high-voltage output circuit enhances power efficiency, as demonstrated in Figure 19. At an output voltage of 20 V, the power efficiency achieved in this work reaches 98.1%. Additionally, the functionality was verified at an output voltage of 30 V, as demonstrated in Figure 20. Figure 20 presents a stimulation waveform following impedance matching at a working voltage of 30 V. The maximum voltage across the electrode model in this figure is approximately 25 V. This limitation arises because the fabrication process supports a maximum voltage of 30 V. To prevent chip breakdown from excessive electrode voltage due to fabrication limitations, we did not increase the electrode waveform to its maximum during testing. Stimulation was observed to occur normally at a working voltage of 30 V (with an electrode voltage exceeding 20 V). This chip can operate normally at a voltage of 30 V while maintaining a high level of charge balance.

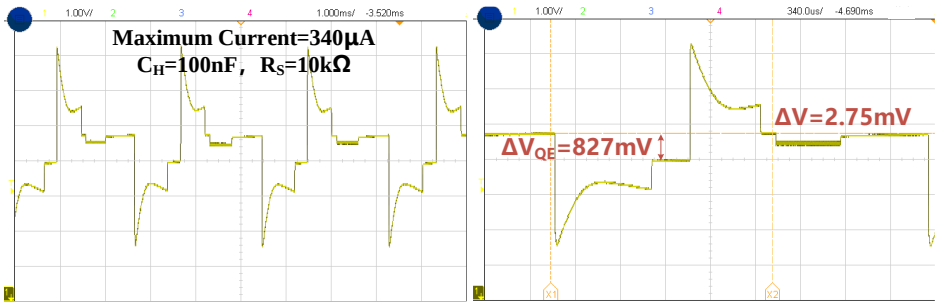

Figure 21. Test under severe current mismatch.

In practical applications, a significant mismatch may occur due to electrode corrosion or changes in the characteristic impedance of the electrode-tissue interface resulting from prolonged stimulation. Figure 21 illustrates the stimulation waveform under conditions of severe exponential current mismatch. There is a notable difference between the anodic stimulation time and the cathodic stimulation time, with a residual charge of 275 pC and a charge mismatch of 0.33%. Furthermore, the short pulse insertion circuit functions properly, and no residual charge accumulated on the electrode exceeds the threshold during multi-cycle stimulation. This demonstrates that the synchronous charge detection system and the short-time pulse insertion circuit can maintain effective charge balance performance even in extreme situations characterized by severe mismatches.

5. In-vitro and in-vivo experiment results

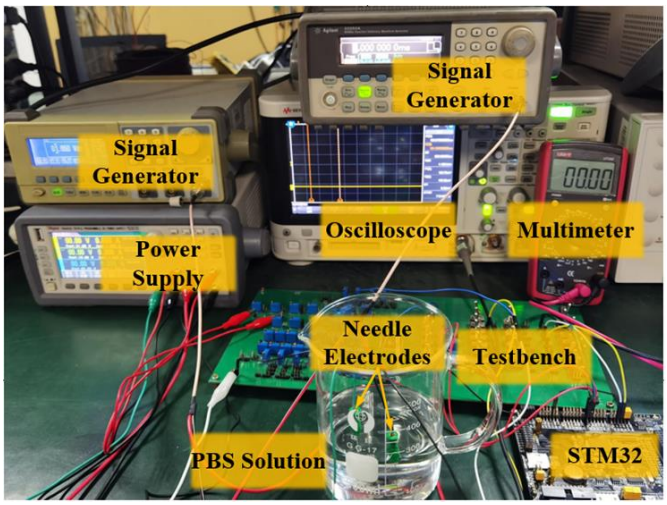

Figure 22. PBS solution testing environment.

Phosphate-buffered saline (PBS) exhibits osmotic pressure and ion concentration comparable to those of the human body; thus, it is employed to simulate the neural tissue environment for chip testing. Figure 22 illustrates the testing environment for the PBS assessment. In comparison to bench-top measurements, two concentric needle electrodes were utilized for testing, with one stimulating electrode immersed in PBS and the other connected to the off-chip reference voltage (V_{REF}).

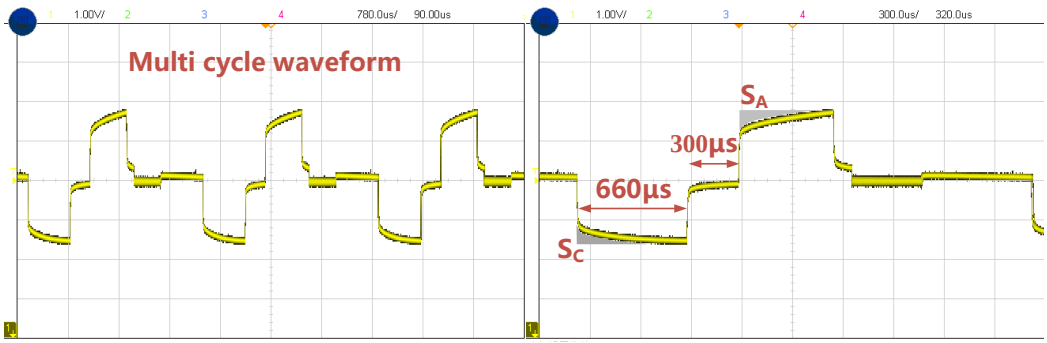

Figure 23. Testing with PBS solution using constant current stimulation.

Figure 23 illustrates the waveform of constant-current stimulation in PBS solution. The test results indicate that under constant current stimulation, the electrode voltage exhibits a significant accumulation effect, suggesting that power efficiency in neural tissue stimulation is lower with this method. The shaded area in Figure 23 corresponds to the heat loss depicted in Figure 3. Amplifying the single-cycle waveform reveals that the insertion time of the short-timepulse is approximately 350 μs (the maximum short-time pulse insertion time is about 500 μs), indicating minimal charge accumulation during single-cycle stimulation. The synchronous charge detection circuit exhibits effective charge control capabilities. The stable electrode voltage observed during multiple cycles confirms the effectiveness of the short-time pulse insertion circuit in removing residual charge.

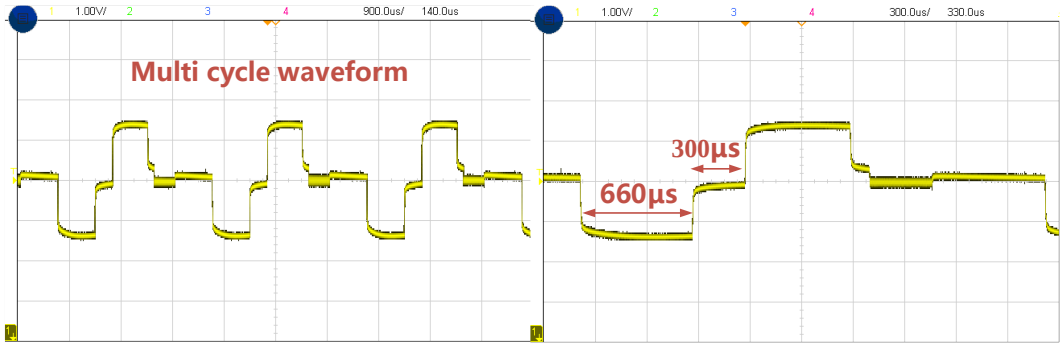

Figure 24. Testing with PBS solution using exponential current stimulation.

Figure 24 presents the test results of exponential-current stimulation in PBS. The pulse width is set at 660 μs, with an interphase delay of 300 μs. The waveform on the right is an enlarged representation of a single cycle derived from the continuous waveform on the left. This indicates that the cathode and anode achieve effective impedance matching. The operation of the short-time pulse insertion circuit remains below its maximum threshold, demonstrating the effectiveness of the synchronous charge detection circuit in balancing charges. Simultaneously, during multi-cycle stimulation, the electrode voltage rapidly recovers to a safe range without significant residual charge, confirming the effective operation of the short-time pulse insertion circuit. During PBS testing, some short-time pulses may still occur even after the residual charge has been removed. This phenomenon results from environmental noise generated during testing, which triggers the voltage detection circuit; however, the electrode voltage ultimately returns to the reference voltage. In summary, the combination of charge matching and charge balancing implemented in this chip demonstrates effective charge control capabilities, ensuring safety during prolonged operation.

6. Animal experiments

We adhered to the ARRIVE guidelines in conducting this animal experiment. The study was performed in full compliance with national and institutional regulations, and ethical approval was obtained from the Medical Experimental Animal Center of Tianjin University of Traditional Chinese Medicine on June 17, 2024 (Approval Number: TCM-LAEC2024058w0919).

Figure 25 illustrates the experimental setup designed for animal experiments, wherein the stimulator delivers stimulation to rats through needle electrodes. This study primarily conducted two animal experiments. The first experiment involved stimulating the rat's vagus nerve using the stimulator while capturing the stimulation waveform with an oscilloscope. The second experiment involved stimulating the rat's sciatic nerve and recording its behavioral response post-stimulation.

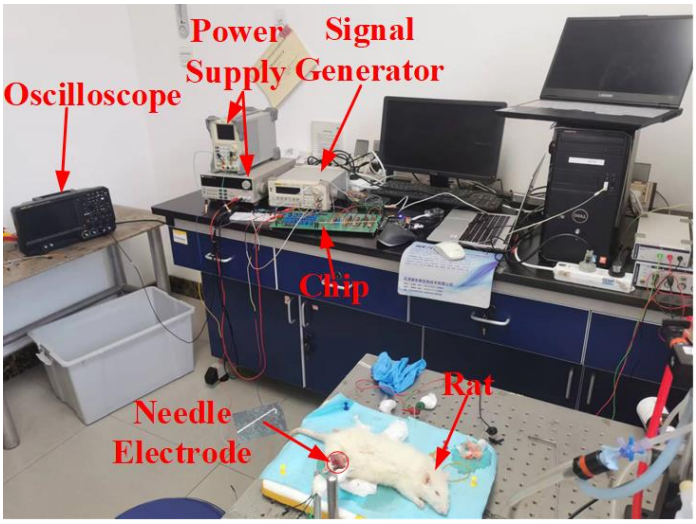

Figure 25. Animal experiment test environment.

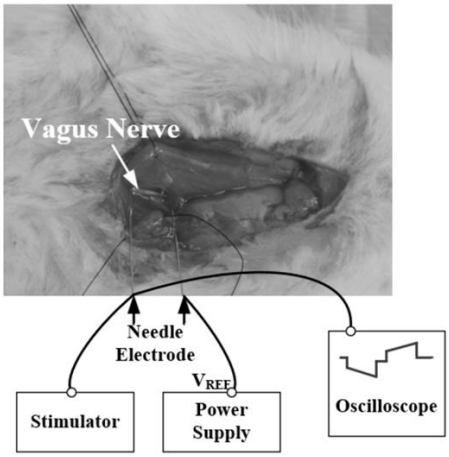

Figure 26. Vagus nerve stimulation configuration.

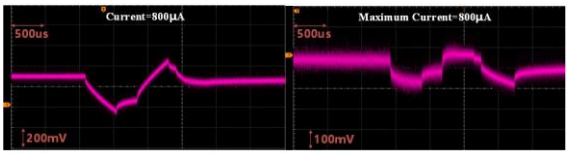

Figure 27. Vagus nerve stimulation waveform.

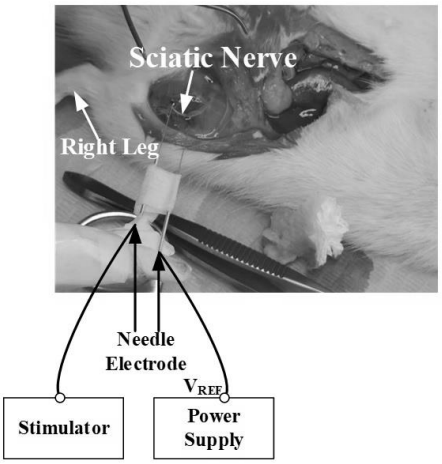

Figure 28. Sciatic nerve stimulation configuration.

Figure 26 illustrates the experimental setup designed for stimulating the vagus nerve of anesthetized rats. The stimulation current produced by the stimulator is delivered to the rat's vagus nerve via a needle electrode. Following a period of vagus nerve stimulation, the current exits through another needle electrode to the reference voltage (VREF). For each stimulation cycle, the stimulation current was set to 800 μA, with the cathode time and anode time both set to 500 μs, and the interphase delay established at 300 μs. [8] Figure 27 presents the stimulation waveform on the vagus nerve; the left side depicts a constant current stimulation waveform, while the right side illustrates an exponential current stimulation waveform. Given the small size of the needle electrodes and the low impedance of the rat vagus nerve, the voltage changes under 800 μA stimulation is minimal; however, the functional potential can still be triggered, allowing for both constant current and exponential current stimulation to be achieved.

In the second animal experiment, this study stimulated the sciatic nerve of anesthetized rats, observing and recording their responses. Figure 28 illustrates the *in vivo* experimental setup used for stimulating the sciatic nerve of anesthetized rats. The sciatic nerve is stimulated with electrical current delivered through needle electrodes to evoke action potentials in the rat's legs. Observations from the experiment indicated that when the sciatic nerve of a rat was stimulated at 800 μA and 100 Hz, the rat's leg muscles contracted vigorously, resulting in noticeable leg movement. When stimulated at a lower frequency of 20 Hz, the rat's leg undergoes a process of stretching to curling, and after curling, it exhibits slight back-and-forth shaking at a set frequency.

Table 1 presents a summary and comparison of the performance of this study with other related research. It is evident that the integrated circuit (IC) achieved the highest output power efficiency while simultaneously incorporating charge balancing and maintaining high output voltage compliance. This work achieved higher stimulation voltages and power efficiency while demonstrating effective charge balance performance. Additionally, it successfully implemented multiple stimulation modes, including both exponential and constant current.

Table 1. Comparison with previous works

Reference	TBCAS'21 [22]	TBCAS'23 [20]	JSSC'22 [13]	TBCAS'17 [11]	JSSC'18 [5]	This work
Technology	180 nm	180 nm	180 nm HV	180 nm	350 nm HV	180 nm BCD
Channels	16	4	16/4	8	1	8
Power supply	±6 V	1.8V/3.3V	40 V	3.3 V	22 V	30V
Core area	2.28 mm^2	1.93 mm^2	30.25 mm^2	2.25 mm^2	1.94 mm^2	8.17 mm^2
Waveform	Square	Exp/Square	Square	Square	Square	Exp/Square
Pulse width	-	≤700 μs	-	-	≤1 ms	≤1 ms
Max. current	3 mA	630 μA	12.75 mA	250 μA	5.12 mA	1 mA
Power efficiency	-	91.3%	-	-	-	98.1%
Charge balancing	Passive charge balancing	Synchronous charge balance and short-time pulse insertion	Time-based charge balancing	Current calibration	Inter-Pulse charge control and offset compensation	Synchronous charge balance and short-time pulse insertion
Residual charge	1.056 nC	255 pC	≤1.76nC (±2 mV)	-	≤2 nC (±20 mV)	2.9 nC
Charge mismatch	0.98%	0.365%	< 1.5%	0.3%	-	0.77%
Charge balance time	≤2 ms	≤60 μs	≤6 ms	3 μ-30 mse	0.3 ms-9 ms	≤500 μs

7. Conclusions

This work presents the design and implementation of a high-voltage, 8-channel neural stimulator chip capable of delivering exponential-waveform currents. A specialized high-voltage output driver has been developed to ensure adequate charge injection at high-impedance electrode-tissue interfaces. By incorporating a synchronous charge detection circuit, the remaining charge after a single stimulation cycle is minimized to only 0.77%. The chip achieves a power efficiency of up to 98% at a supply voltage of 20 V and can operate at a maximum voltage of 30 V. Additionally, effective charge balancing is maintained during multi-cycle stimulation, with charge balancing circuits compatible with both the exponential-waveform generation circuit and the high-voltage output stages. Bench-top measurements and *in vitro* experiments have demonstrated the superior power efficiency of the chip. Furthermore, the neural stimulation chip has successfully undergone *in vivo* testing on rats. This proposed 8-channel high-voltage neural stimulator holds potential applications in neural modulation, brain-machine interface (BMI) systems, and other biomedical devices.

Acknowledgment

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Conflicts of interests

The author declares no conflict of interest.

Ethical statement

We adhered to the ARRIVE guidelines in conducting this animal experiment. The study was performed in full compliance with national and institutional regulations, and ethical approval was obtained from the Medical Experimental Animal Center of Tianjin University of Traditional Chinese Medicine on June 17, 2024 (Approval Number: TCM-LAEC2024058w0919).

Authors' contribution

Conceptualization and design:Xu Liu, Zeyu Lu, Juzhe Li; methodology: Xu Liu, Juzhe Li; software and validation: Zeyu Lu, Weijian Chen; formal analysis: Biao Sun, Jiaqi Sun; investigation and data curation: Shenjun Wang, Xue Zhao, Lin Zheng; resources: Shenjun Wang, Xue Zhao, Lin Zheng; writing and original draft preparation: Zeyu Lu, Weijian Chen; writing, review and editing: Biao Sun, Jiaqi Sun, Gengchen Sun; supervision: Hao Yu, Liuyang Zhang; project administration: Xu Liu, Biao Sun, Shenjun Wang, Hao Yu, Liuyang Zhang, Gengchen Sun. All authors have read and agreed to the published version of the manuscript.

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